ECE 448
Lecture 6

Finite State Machines

State Diagrams
vs.
Algorithmic State Machine (ASM) Charts

Required reading

- P. Chu, *FPGA Prototyping by VHDL Examples*

  Chapter 5, FSM

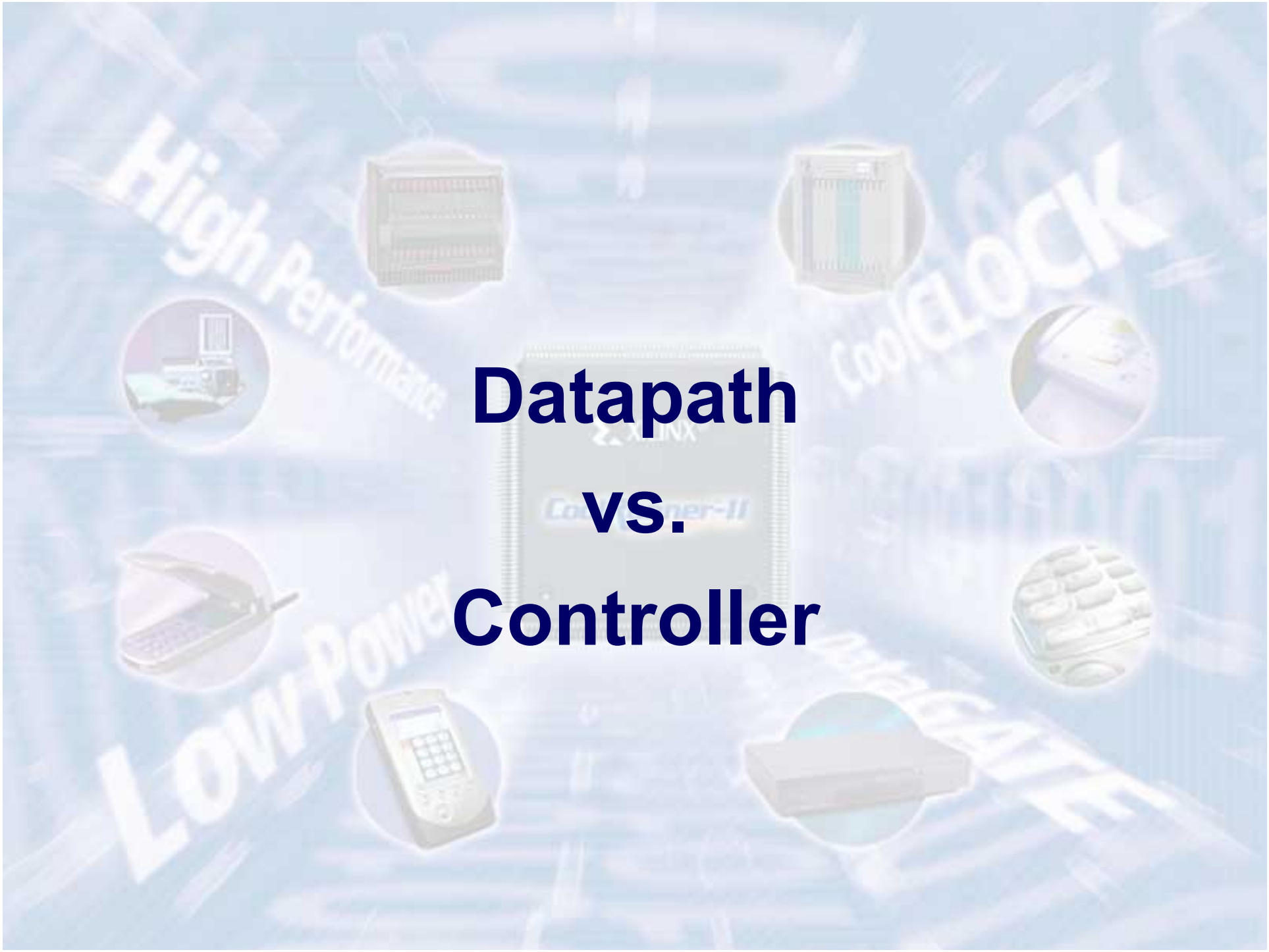
Recommended reading

- S. Brown and Z. Vranesic,
  Fundamentals of Digital Logic with VHDL Design

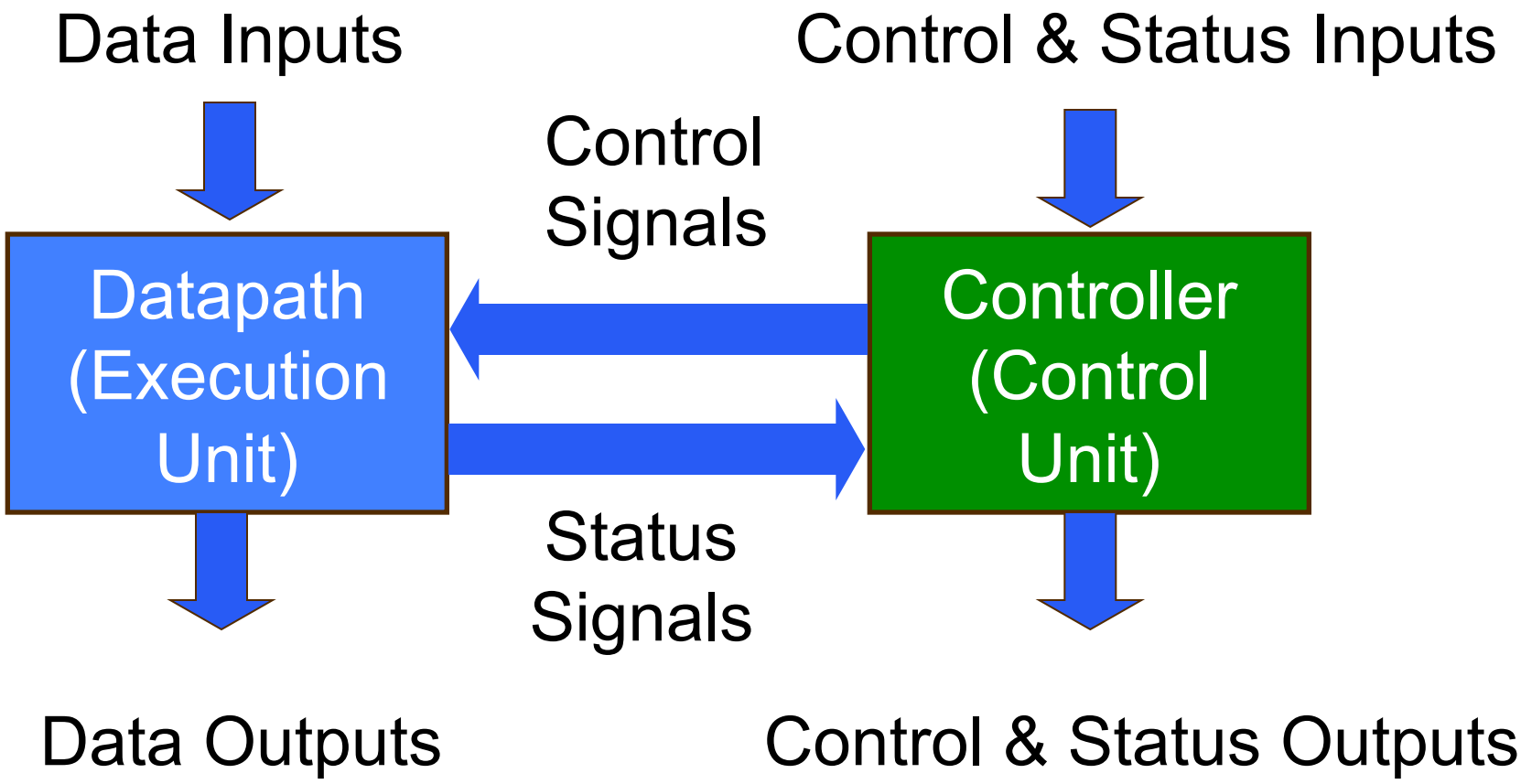
  Chapter 8, Synchronous Sequential Circuits

  Sections 8.1-8.5

  Section 8.10, Algorithmic State Machine (ASM) Charts


Datapath
vs.
Controller

Structure of a Typical Digital System



Datapath (Execution Unit)

- Manipulates and processes data
- Performs arithmetic and logic operations, shifting/rotating, and other data-processing tasks
- Is composed of registers, multiplexers, adders, decoders, comparators, ALUs, gates, etc.
- Provides all necessary resources and interconnects among them to perform specified task
- Interprets control signals from the Controller and generates status signals for the Controller

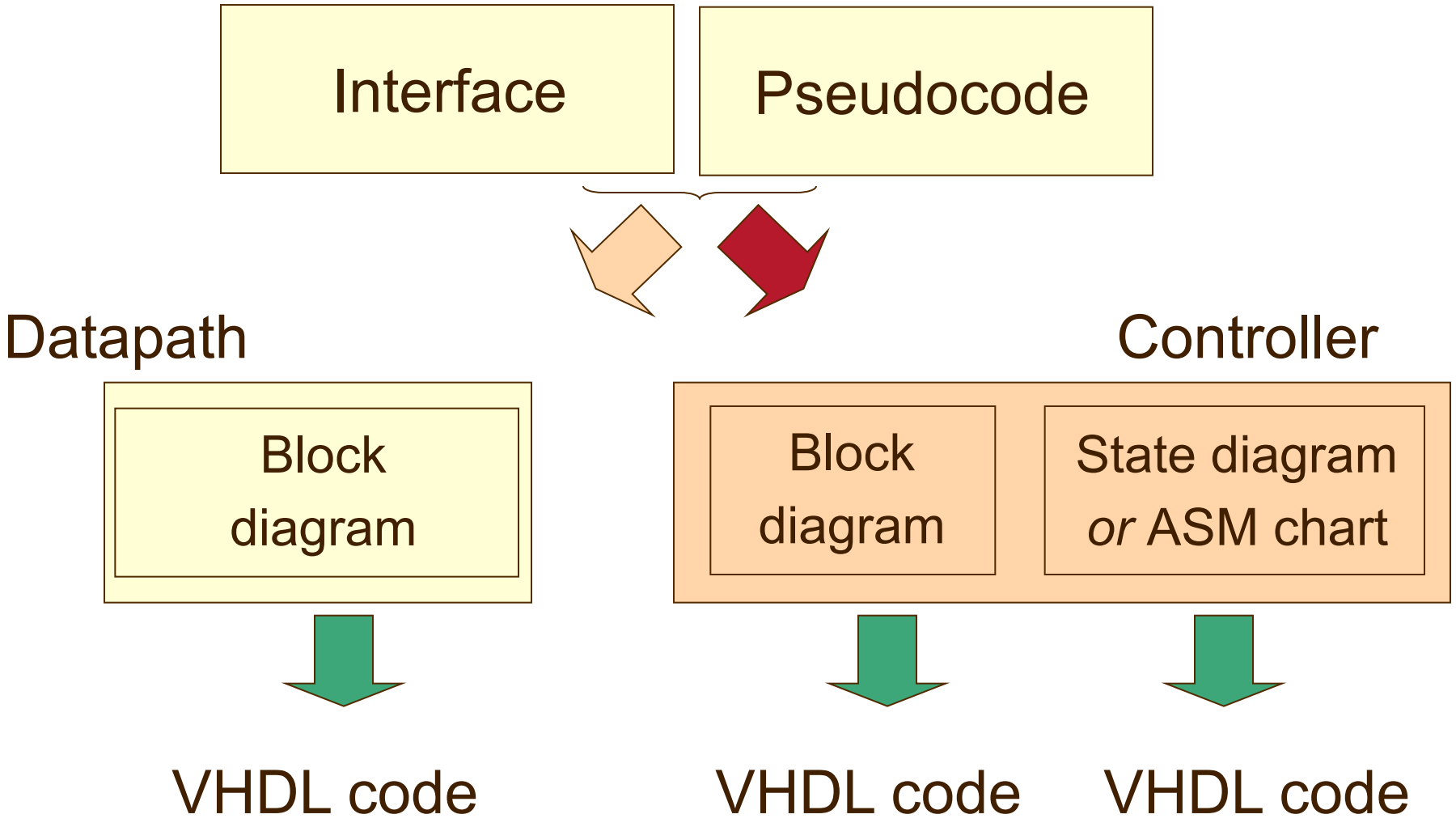
Controller (Control Unit)

- Controls data movement in the Datapath by switching multiplexers and enabling or disabling resources
  - Example: enable signals for registers
  - Example: select signals for muxes
- Provides signals to activate various processing tasks in the Datapath
- Determines the sequence of operations performed by the Datapath
- Follows Some ‘Program’ or Schedule

Finite State Machines

- Controllers can be described as Finite State Machines (FSMs)
- Finite State Machines can be represented using
  - **State Diagrams and State Tables** - suitable for simple controllers with a relatively few inputs and outputs
  - **Algorithmic State Machine (ASM) Charts** - suitable for complex controllers with a large number of inputs and outputs
- All of these descriptions can be easily translated to the corresponding synthesizable VHDL code

Hardware Design with RTL VHDL



Steps of the Design Process

1. Text description
2. Interface
3. Pseudocode
4. Block diagram of the Datapath
5. Interface divided into Datapath and Controller
6. State diagram or ASM chart of the Controller
7. RTL VHDL code of the Datapath, Controller, and Top-Level Unit
8. Testbench for the Datapath, Controller, and Top-Level Unit
9. Functional simulation and debugging
10. Synthesis and post-synthesis simulation
11. Implementation and timing simulation
12. Experimental testing using FPGA board

Steps of the Design Process Introduced in Class Today

1. Text description
2. Interface
3. Pseudocode
4. Block diagram of the Datapath
5. Interface divided into Datapath and Controller
6. **State diagram or ASM chart of the Controller**
7. **RTL VHDL code of** the Datapath, **Controller**, and Top-level Unit
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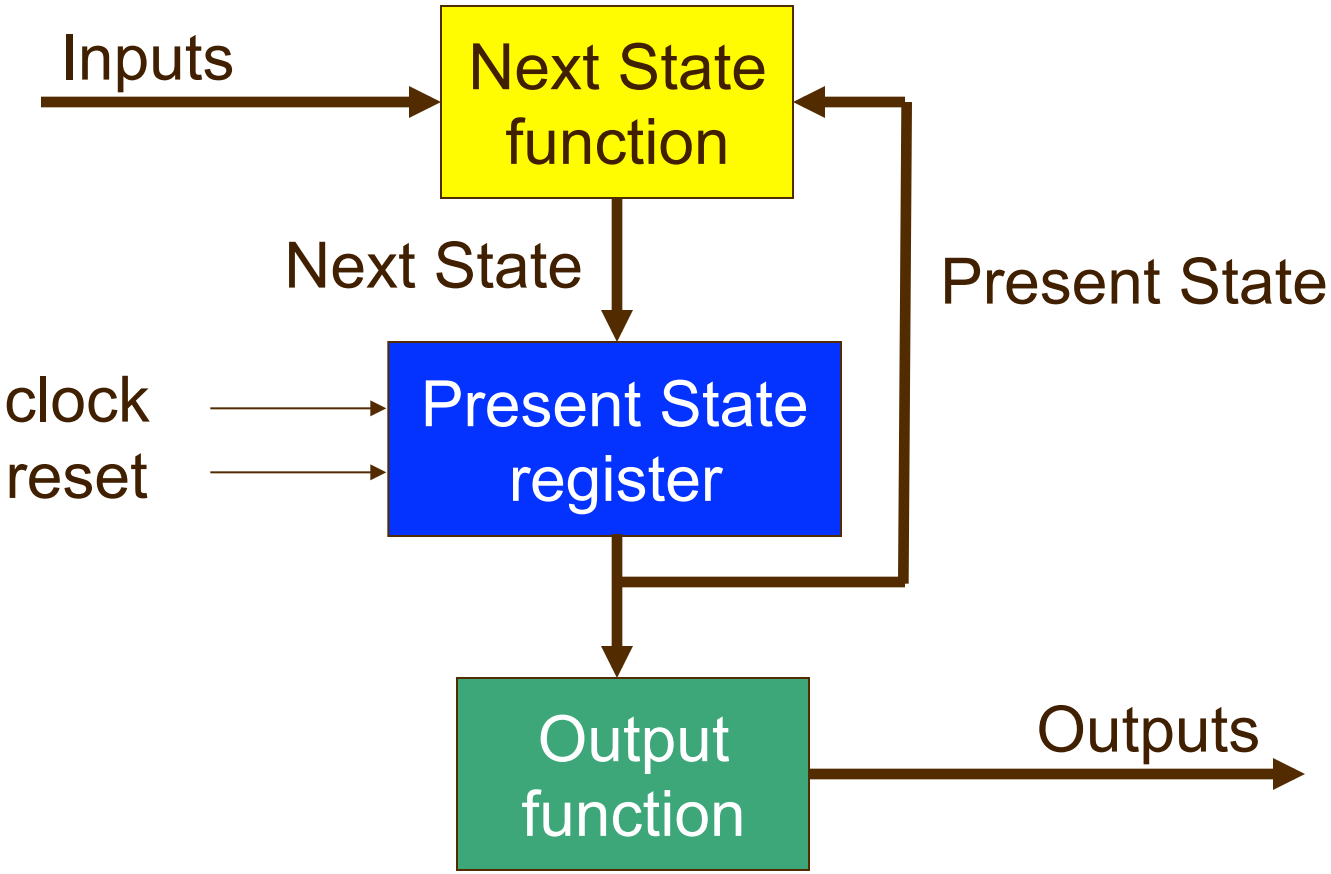
Finite State Machines Refresher

Finite State Machines (FSMs)

- An FSM is used to model a system that transits among a finite number of internal states. The transitions depend on the current state and external input.
- The main application of an FSM is to act as the controller of a medium to large digital system
- Design of FSMs involves
  - Defining states
  - Defining next state and output functions
  - Optimization / minimization
- Manual optimization/minimization is practical for small FSMs only

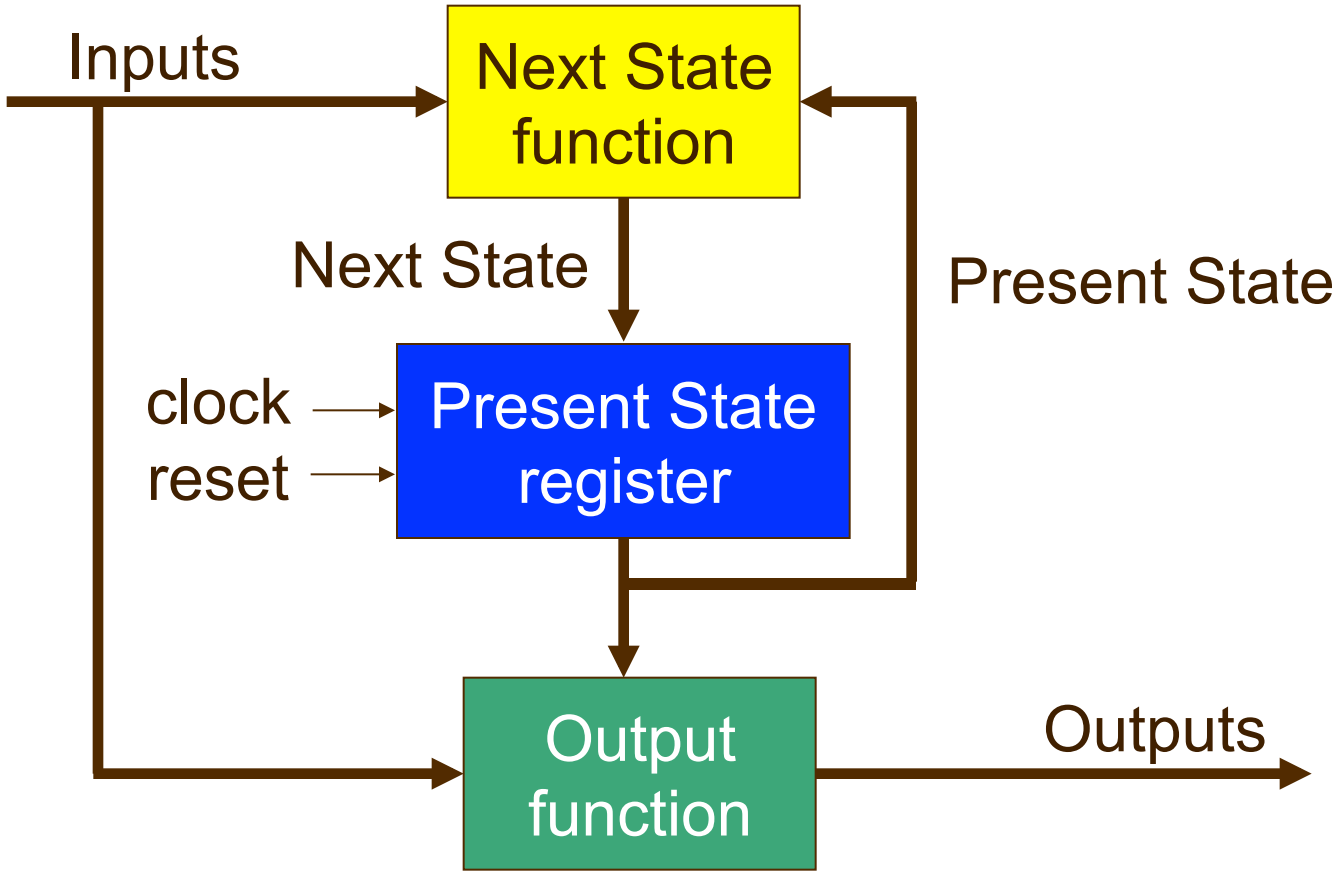
Moore FSM

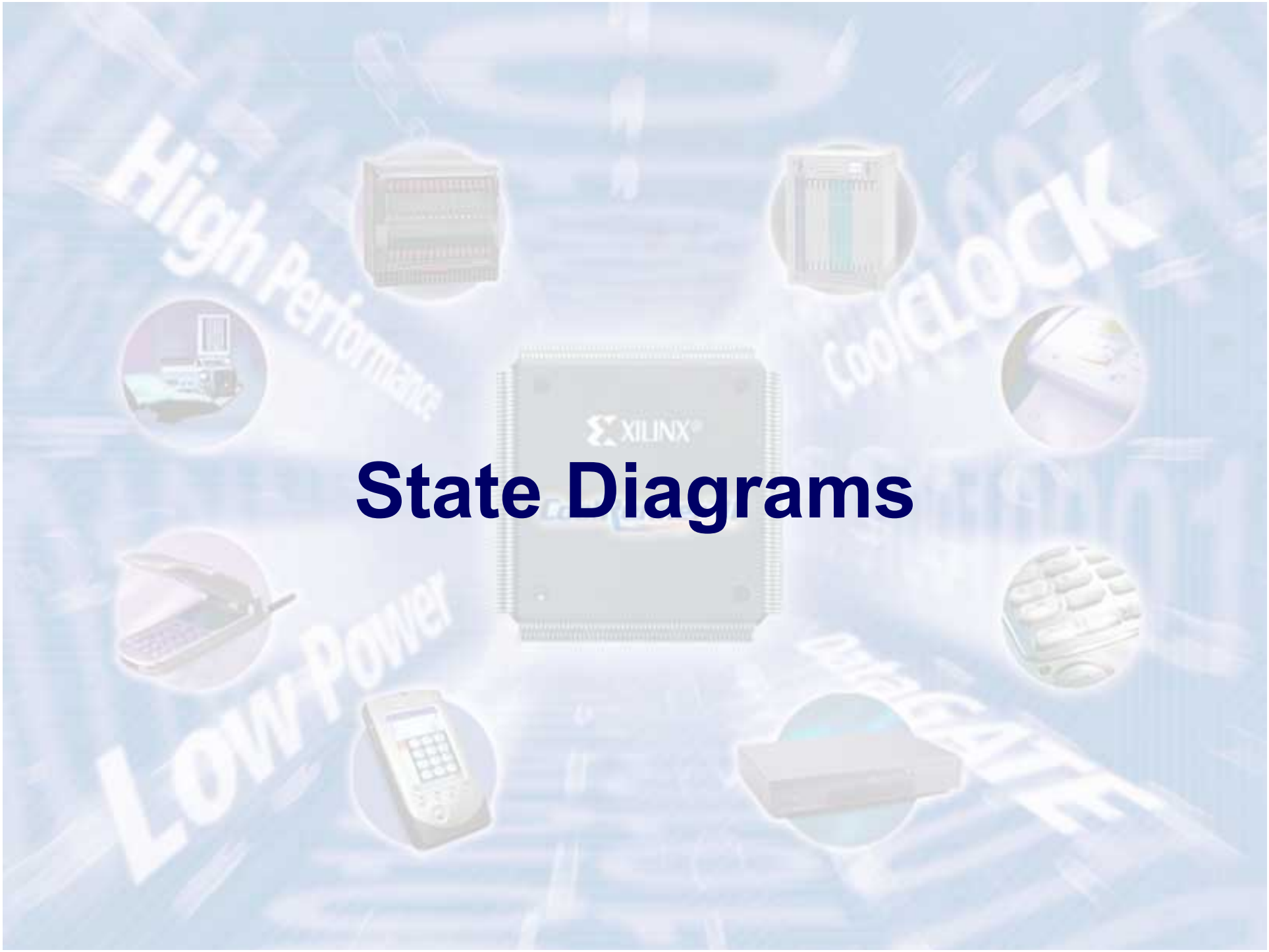
- Output is a Function of the Present State Only



Mealy FSM

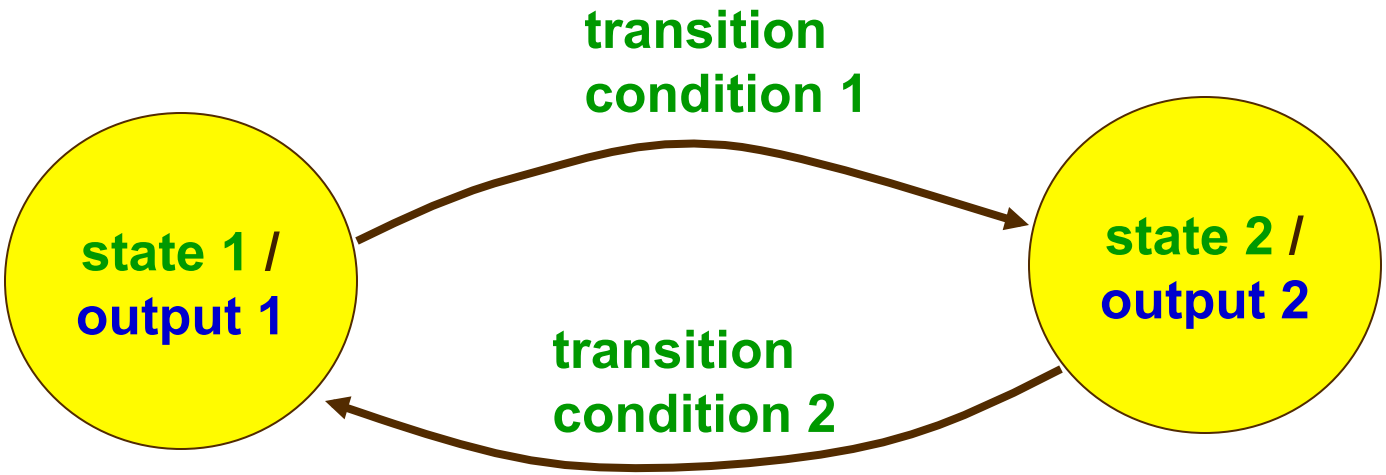
- Output is a Function of the Present State and the Inputs



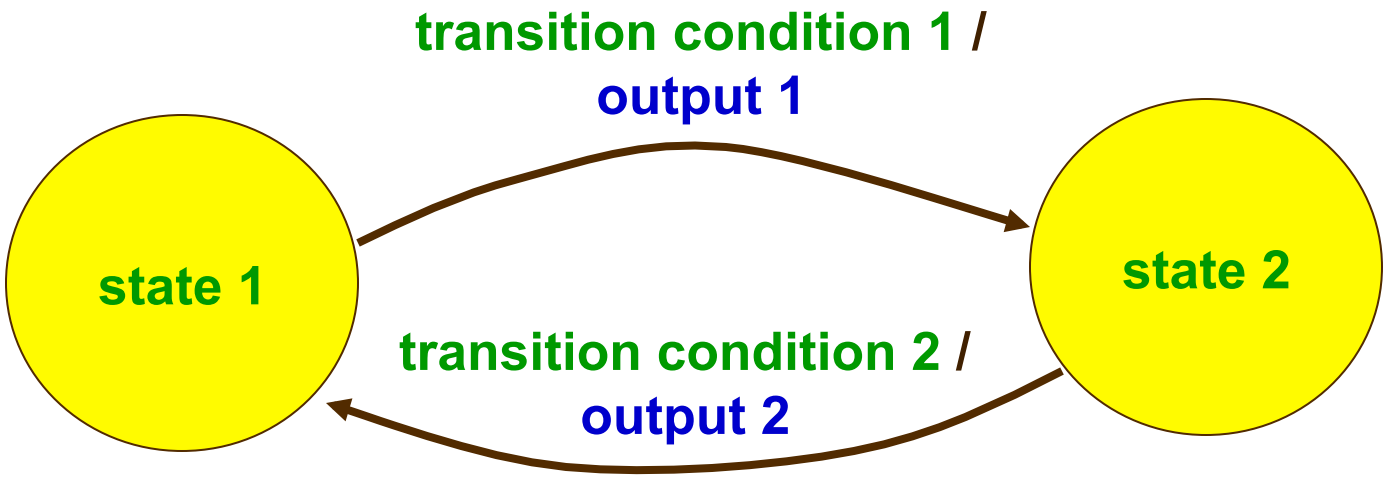


State Diagrams

Moore Machine

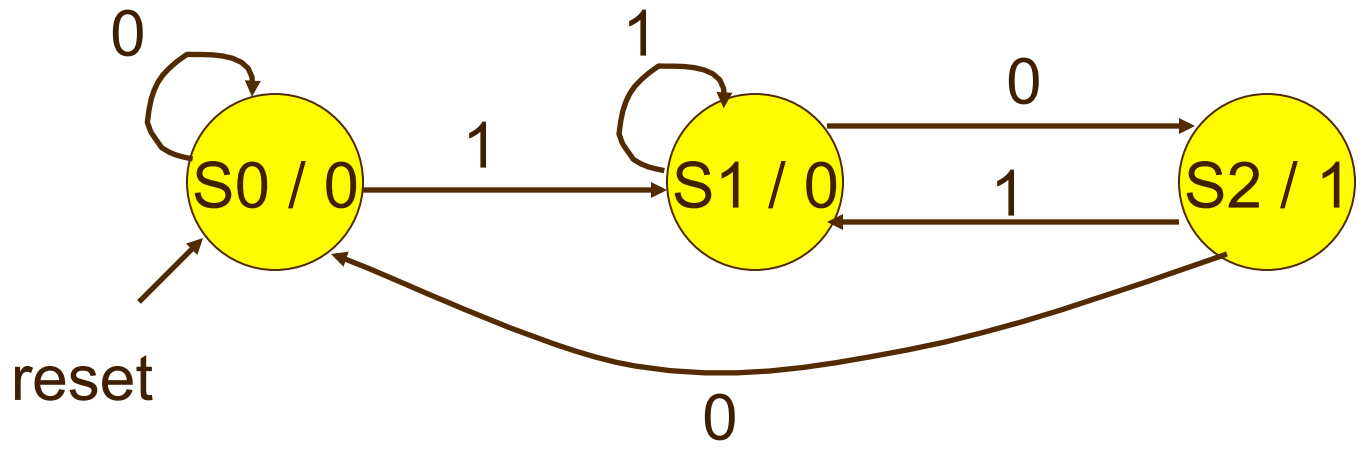


Mealy Machine



Moore FSM - Example 1

- Moore FSM that Recognizes Sequence “10”



Meaning of states:

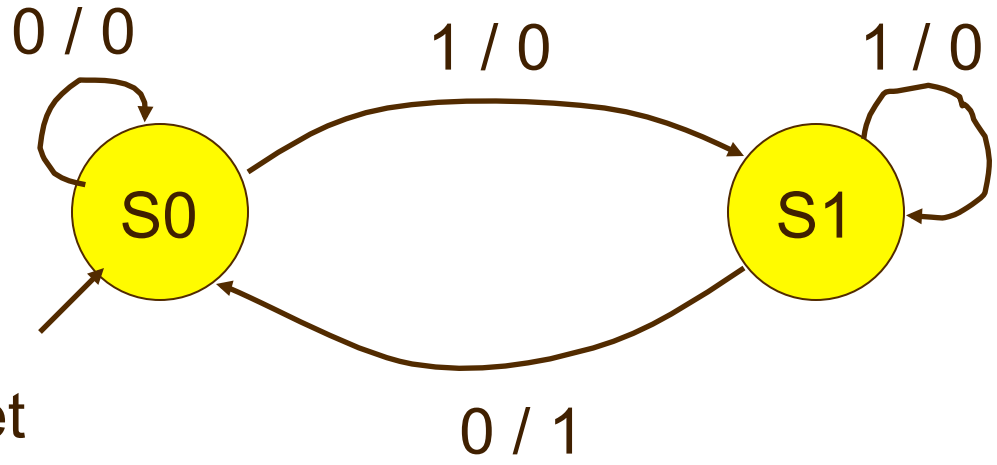
S0: No elements of the sequence observed

S1: “1” observed

S2: “10” observed

Mealy FSM - Example 1

- Mealy FSM that Recognizes Sequence "10"



Meaning of states:

S0: No elements of the sequence observed

S1: "1" observed



Algorithmic State Machine (ASM) Charts

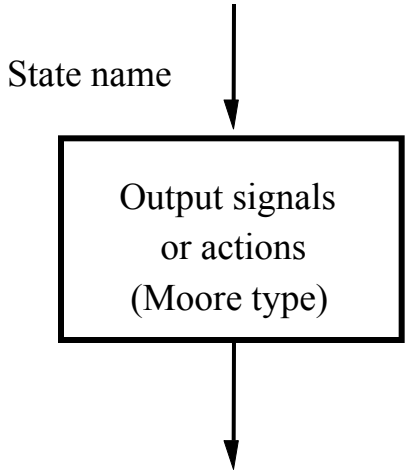
Algorithmic State Machine

Algorithmic State Machine –

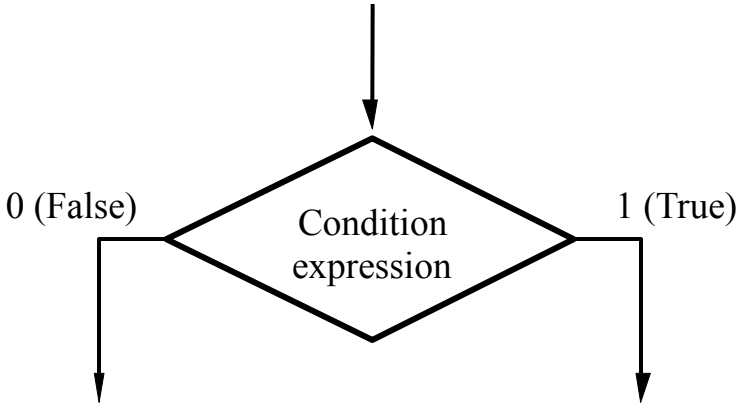
representation of a Finite State Machine

suitable for FSMs with a larger number of inputs and outputs compared to FSMs expressed using state diagrams and state tables.

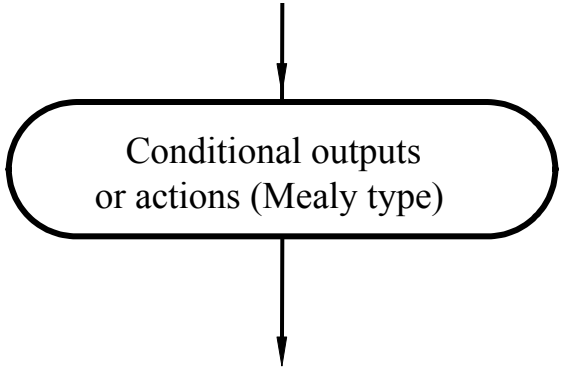
Elements used in ASM charts (1)



(a) State box



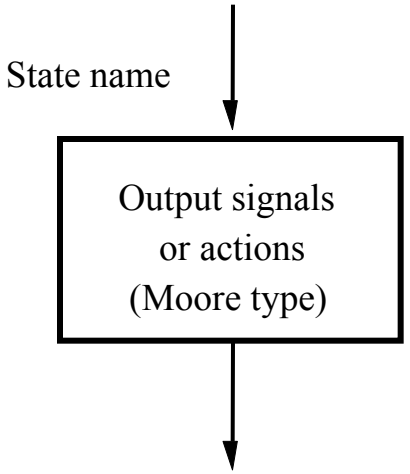
(b) Decision box



(c) Conditional output box

State Box

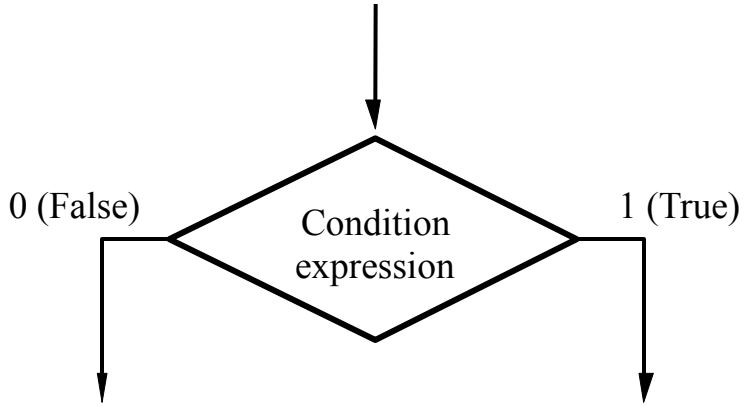
- **State box** – represents a state.
- Equivalent to a node in a state diagram or a row in a state table.
- Contains register transfer actions or output signals
- **Moore-type outputs are listed inside of the box.**
- It is customary to write only the name of the signal that has to be asserted in the given state, e.g., z instead of z<=1.
- Also, it might be useful to write an action to be taken, e.g., count <= count + 1, and only later translate it to asserting a control signal that causes a given action to take place (e.g., enable signal of a counter).



Decision Box

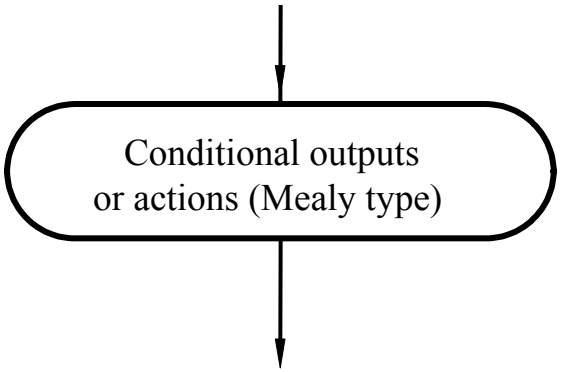
- **Decision box** – indicates that a given condition is to be tested and the exit path is to be chosen accordingly.

  The condition expression may include one or more inputs to the FSM.

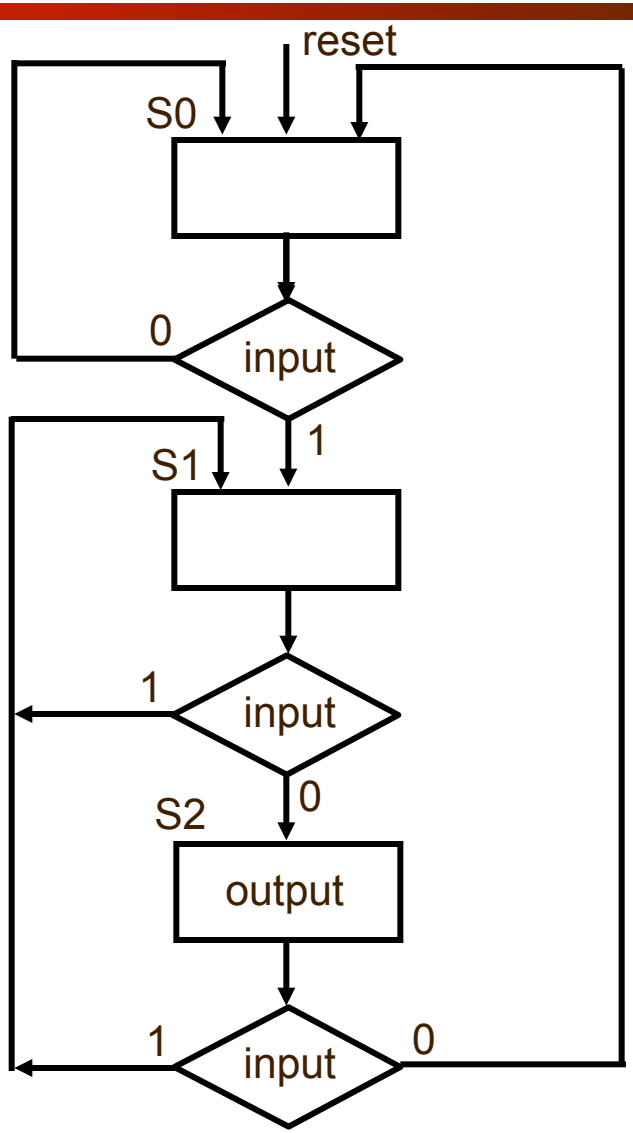


Conditional Output Box

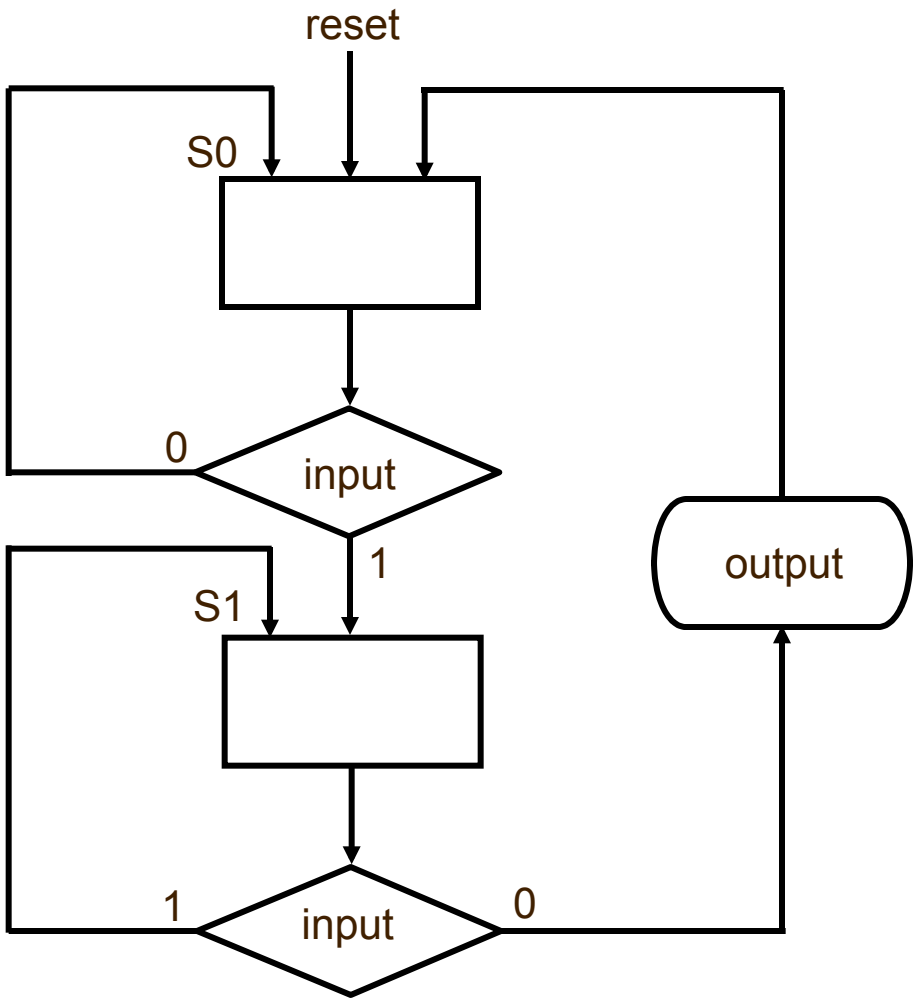
- **Conditional output box**
- Denotes output signals that are of the Mealy type.
- The condition that determines whether such outputs are generated is specified in the decision box.



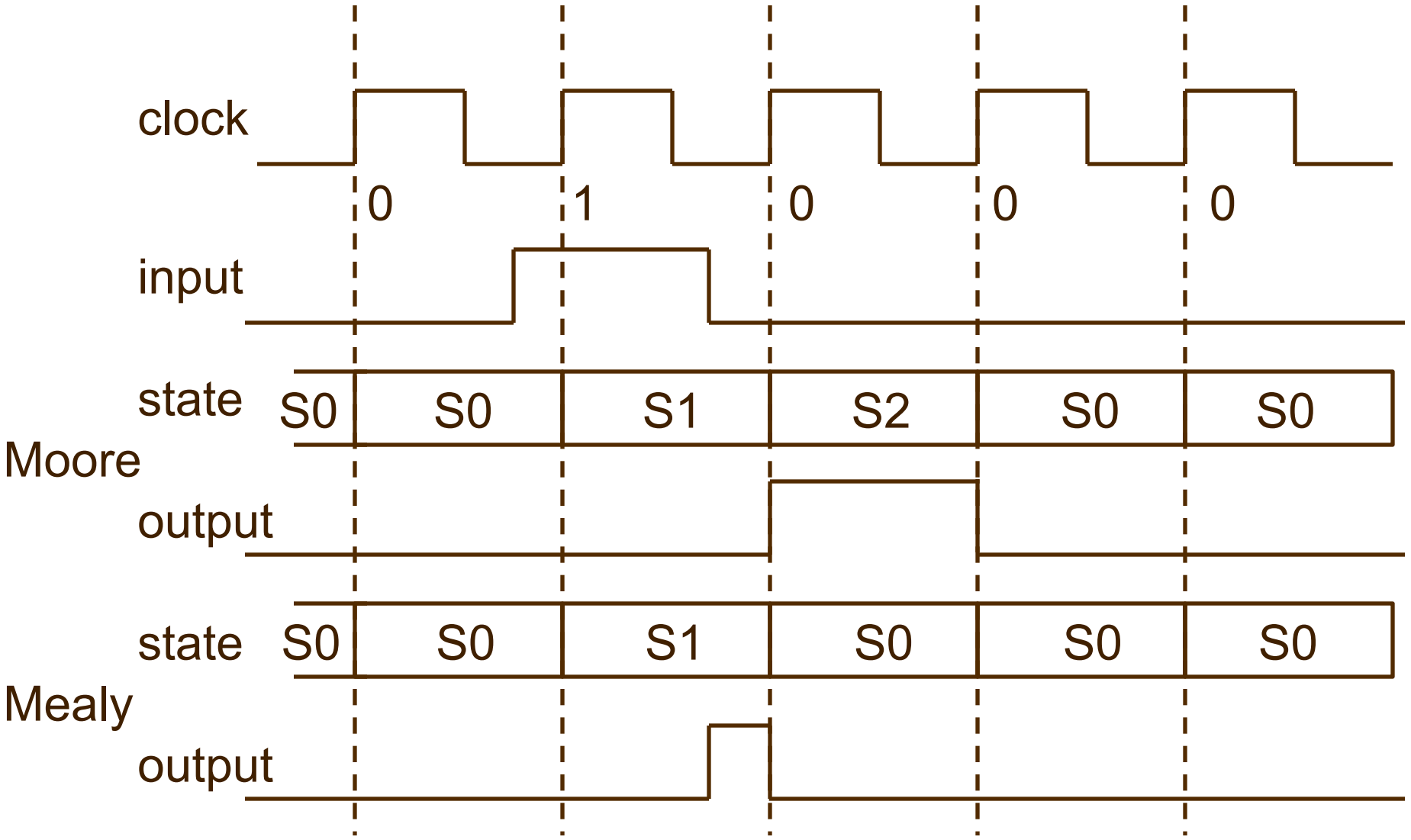
ASM Chart of Moore Machine



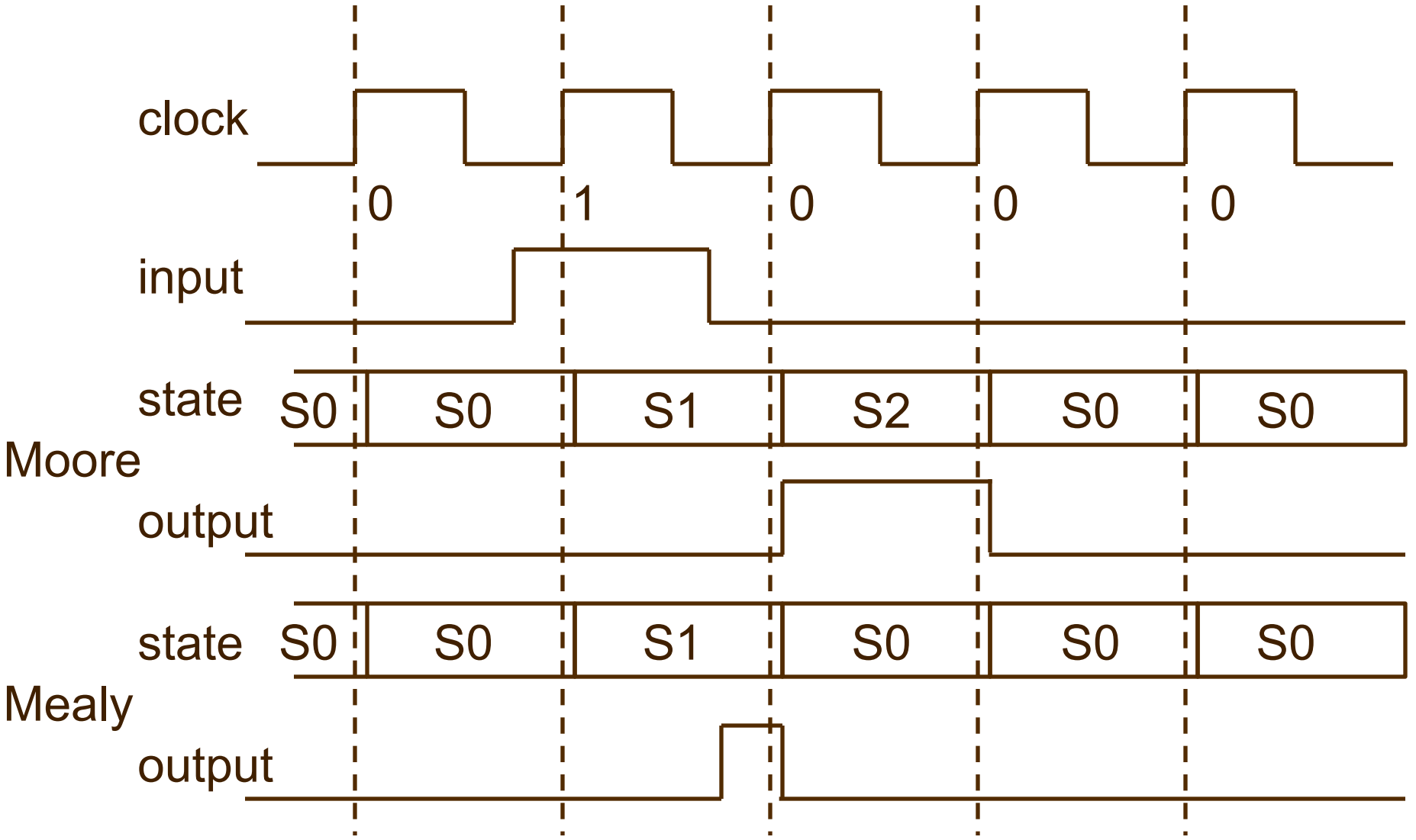
ASM Chart of Mealy Machine



Moore & Mealy FSMs without delays



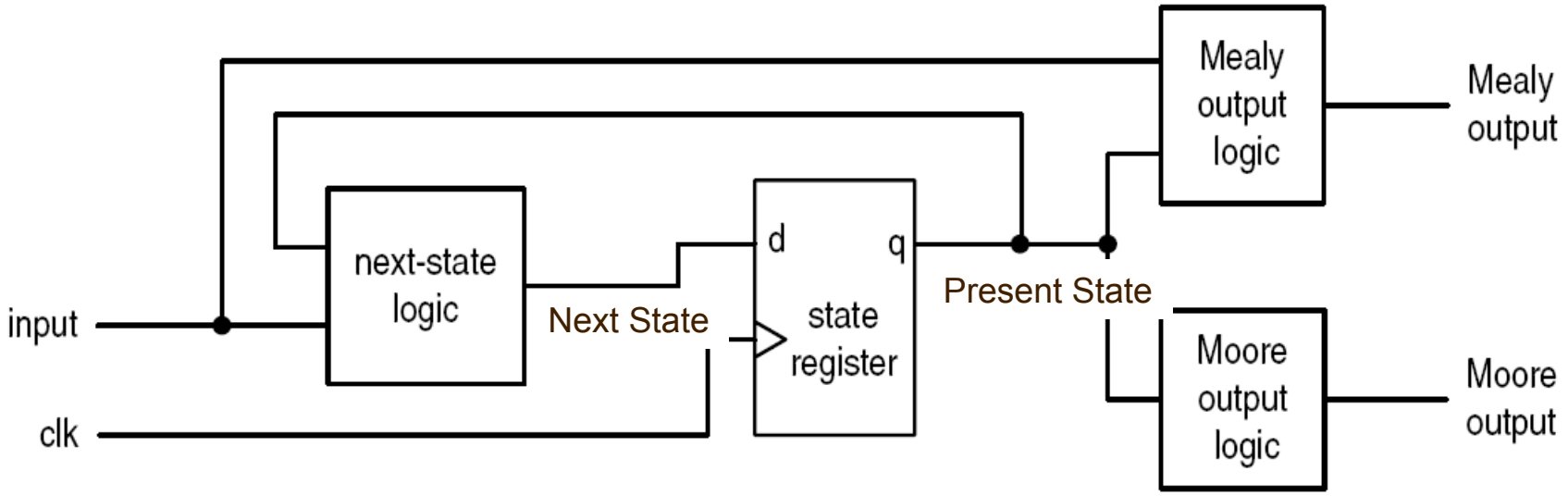
Moore & Mealy FSMs with delays



ASMs representing simple FSMs

- Algorithmic state machines can model both Mealy and Moore Finite State Machines
- They can also model machines that are of the mixed type

Generalized FSM



Based on RTL Hardware Design by P. Chu

Moore vs. Mealy FSM (1)

- Moore and Mealy FSMs Can Be Functionally Equivalent
  - Equivalent Mealy FSM can be derived from Moore FSM and vice versa
- Mealy FSM Has Richer Description and Usually Requires Smaller Number of States
  - Smaller circuit area

Moore vs. Mealy FSM (2)

- Mealy FSM Computes Outputs as soon as Inputs Change
  - Mealy FSM responds one clock cycle sooner than equivalent Moore FSM
- Moore FSM Has No Combinational Path Between Inputs and Outputs
  - Moore FSM is less likely to affect the critical path of the entire circuit

Moore vs. Mealy FSM (3)

- Types of control signal
  - Edge sensitive
    - E.g., enable signal of a counter
    - Both can be used but Mealy is faster
  - Level sensitive
    - E.g., write enable signal of SRAM
    - Moore is preferred

Which Way to Go?

Mealy FSM

Fewer states

Lower Area

Responds one clock cycle earlier

Moore FSM

Safer.
Less likely to affect the critical path.

