Final Exam

Final Exam – 25 points

Wednesday, May 9, 1:30pm-4:15pm

Part II – Typical Problems

1. (pseudocode, interface) => block diagram
2. (pseudocode, interface, block diagram) =>
   ASM chart
3. actions => control signals (including “-”)
4. I/O register map and a wrapper that modifies this circuit into an MMIO unit of an FPro system

Part I – Typical Problems

1. fill in the blanks
2. circuits with a regular structure (for-generate)
3. VHDL code => block diagram
4. timing waveforms based on an ASM chart & inputs
5. VGA display system
6. Xilinx FPGA memories
7. FPro Bus Protocol and MMIO Slot Specification
8. Bare Metal System Software Development

Exams from Previous Years

Spring 2008-Spring 2015