

Midterm Exam

**ECE 448
Spring 2007**

Tuesday Section

(15 points)

Instructions

Zip all your deliverables into an archive <last_name>.zip and submit it through WebCT no later than Tuesday, March 20, 10:30 PM EST.

Introduction

Design a digital system that will compute a median for a set of three data inputs of the size of N bits each. The three data inputs are clocked in serially beginning at the high value of the signal START. The median value is generated at the output at the same time as the DONE signal. Reset signal is asynchronous. CLK period is 10ns for simulation. All registers are active on the rising edge of the clock. Assume the default value of N = 8.

The pseudocode for computing the median of three values DATA_IN(1), DATA_IN(2) and DATA_IN(3) is given below:

```
D=DATA_IN(1)
DMAX = D
```

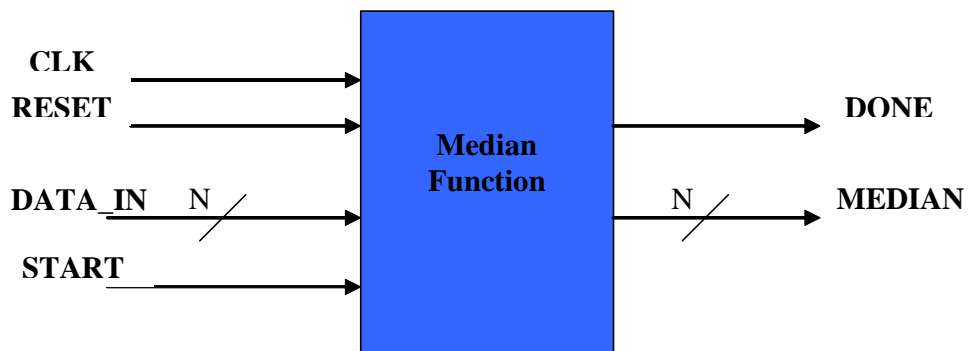
```
D=DATA_IN(2)
if D>DMAX then
  DMED = DMAX
  DMAX = D
else
  DMED = D
end if
```

```
D=DATA_IN(3)
if D>DMAX then
  DMED = DMAX
  DMAX = D
elsif D > DMED
  DMED = D
end if
```

```
MEDIAN = DMED
```

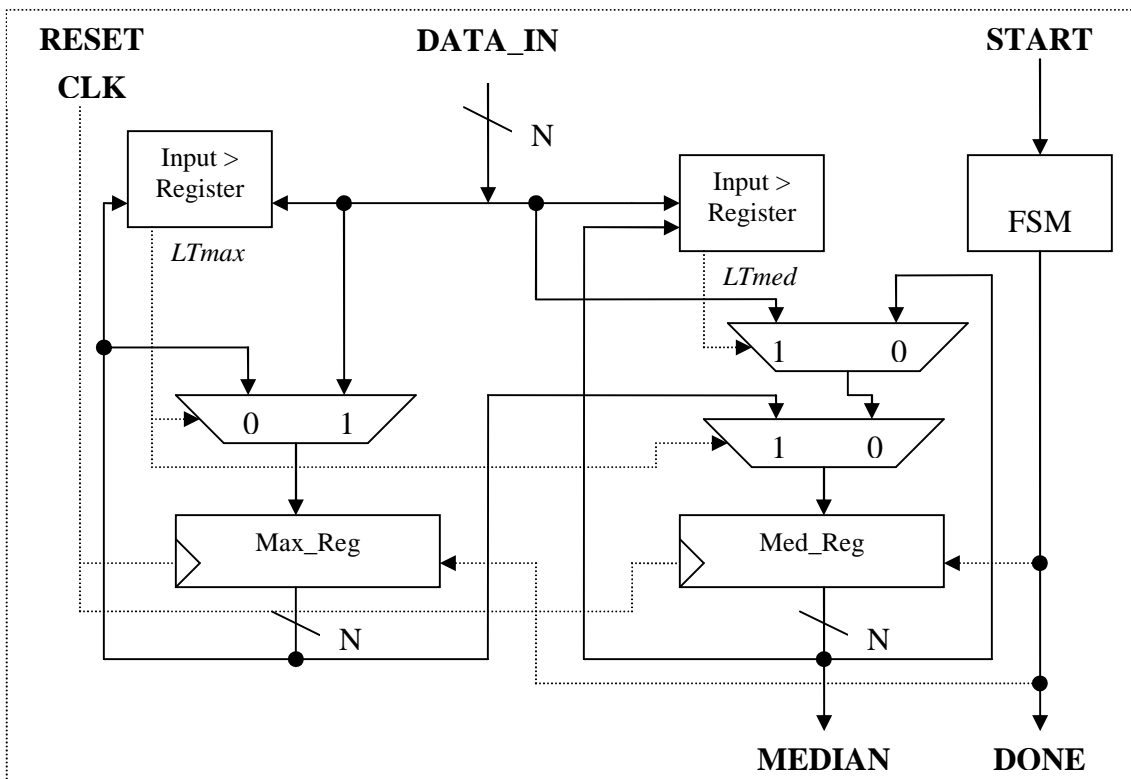
DMAX denotes current maximum
DMED denotes current second value

The interface of the circuit is shown below:

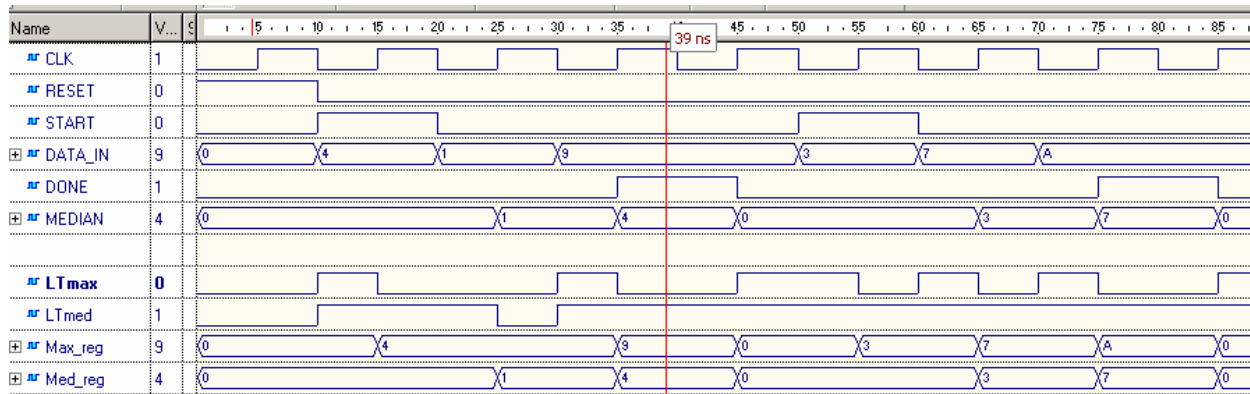


Signal	Mode	Size (bits)	Function
CLK	Input	1	10ns, 50% duty cycle master clock
RESET	Input	1	Asynchronous reset
START	Input	1	Starts the computation cycle, active high for 1 clock cycle
DATA_IN	Input	N	Inputs data points serially for 3 consecutive clock cycles beginning at the high value of the START signal
MEDIAN	Output	N	Outputs median point
DONE	Output	1	Signals the end of the computation. Output is valid on this signal. This signal also clears both Max and Med registers to get ready for the next computation.

The execution unit of the circuit is described below



The timing waveform is shown below for $N = 4$



Design Requirements

The combinational portion of the circuit should be described using the dataflow VHDL code, and the sequential portion of the circuit should be described using the synthesizable behavioral code. Your code should infer a circuit that requires a minimum amount of FPGA resources. The target clock frequency should be 100 MHz.

Tasks

Perform the following tasks:

1. Write a VHDL code of the execution unit of the described above circuit (shown in the block diagram above).
2. Write a testbench verifying the operation of your execution unit for the case of $N=8$.
3. Perform functional simulation of your circuit and use it to debug your VHDL code.
4. Design a control unit of your circuit. If you do not know how to do it, go to Step 6.
5. Write a testbench verifying the operation of your entire code for the case of $N=8$.
6. Synthesize your circuit using Synplify Pro for the case of $N=8$. Save the RTL schematic.
7. Implement your circuit using Xilinx ISE.
8. Perform timing simulations of your circuit using Active-HDL.
9. Run the static timing analysis of your circuit.
10. Based on the circuit block diagram and the implementation reports, determine the most critical path in your circuit and its length.

Deliverables

1. VHDL code of your entire circuit fulfilling the requirements specified in the Design Requirements section above
2. VHDL code of your testbenches
3. RTL schematic of your circuit
4. Timing waveforms from the functional simulation demonstrating the correct operation of your circuit.
5. Description of the critical path in your circuit
6. Timing waveforms from the timing simulation demonstrating the delay of the circuit most critical path
7. FPGA resource utilization
8. Minimum clock period of your circuit.