Midterm Exam

ECE 448
Spring 2007

Wednesday Section

(15 points)

Instructions
Zip all your deliverables into an archive <last_name>.zip and submit it through WebCT no later than Wednesday, March 21, 10:30 PM EST.

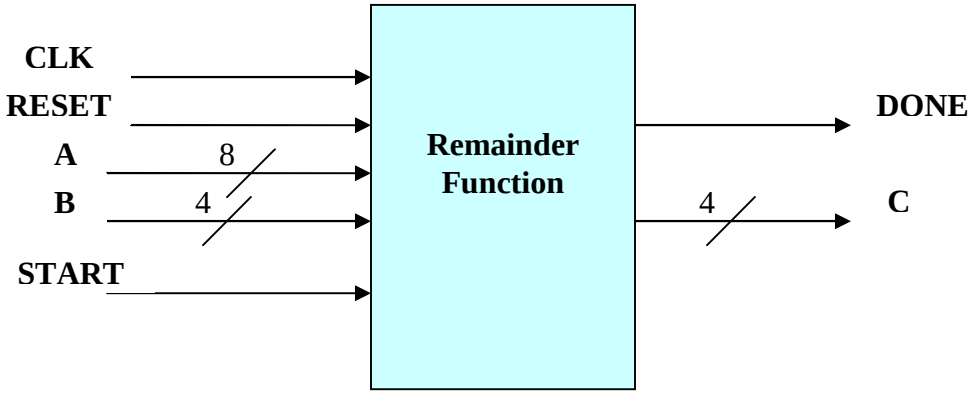
Introduction

Design a digital system that will compute the remainder C = A mod B for the number A in the range from 0 to 255 (i.e., an 8-bit number), and the number B in the range from 8 to 15 (i.e., a 4-bit number with the most significant bit set to 1). The data inputs are clocked in at high value of the START signal. The remainder value is generated at the output at the same time as the DONE signal. RESET signal is asynchronous. CLK period is 20ns for simulation. All registers are active on the rising edge of the clock.

The pseudocode for computing the remainder of A modulo B is given below:

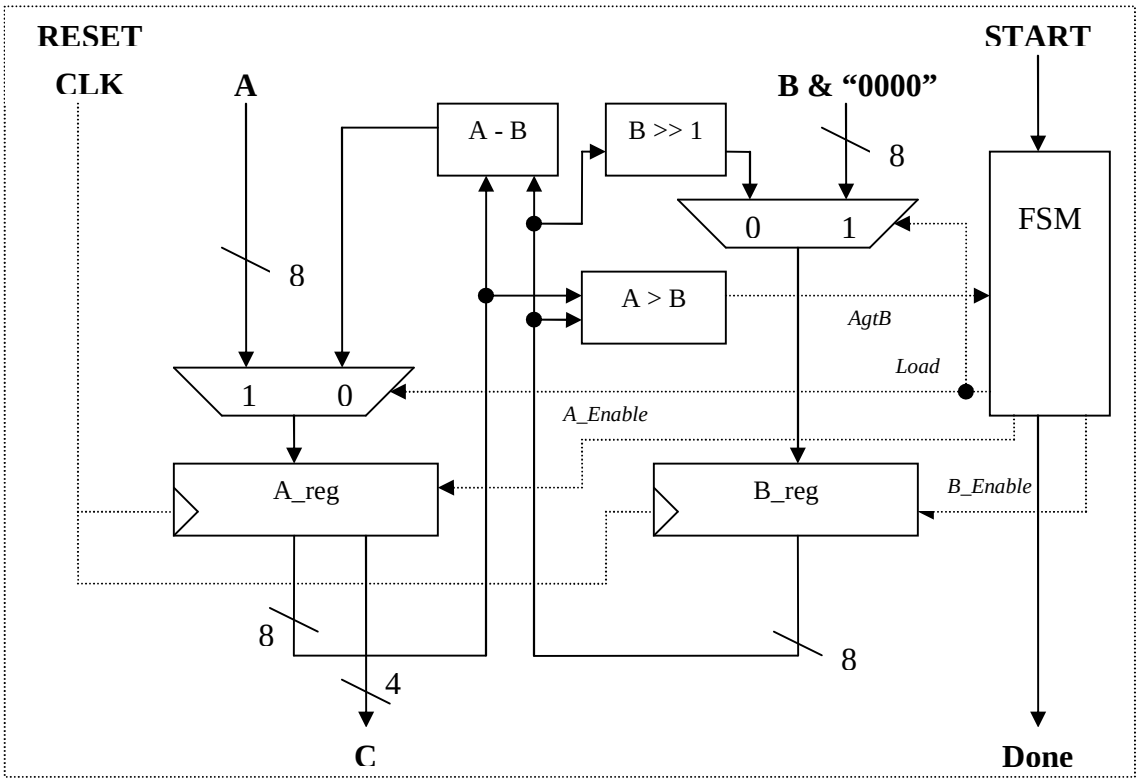
```
A_reg = A
B_reg = B*2^4
for i = 0 to 4 do
  if A_reg > B_reg
    A_reg = A_reg – B_reg
  end if
  B_reg = B_reg >> 1
end for
C = A_reg[3 downto 0]
```

The interface of the circuit is shown below:

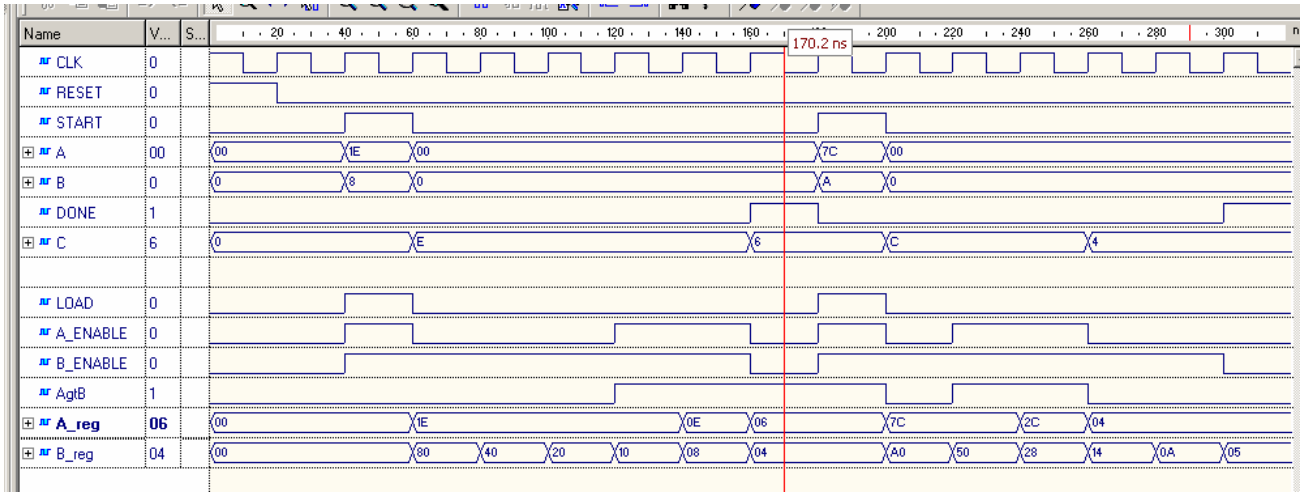


Signal	Mode	Size (bits)	Function
CLK	Input	1	20ns, 50% duty cycle master clock
RESET	Input	1	Asynchronous reset
START	Input	1	Starts the computation cycle, active high for one clock cycle
A	Input	8	Inputs value A, clocked in during the active value of the START signal
B	Input	4	Inputs value B, clocked in during the active value of the START signal
C	Output	4	C = A mod B (example: 154 mod 10 = 4)
DONE	Output	1	Signals the end of the computation. Output is valid on this signal.

The execution unit of the circuit is described below:



The timing waveform is shown below:



Design Requirements

The combinational portion of the circuit should be described using the dataflow VHDL code, and the sequential portion of the circuit should be described using the synthesizable behavioral code. Your code should infer a circuit that requires a minimum amount of FPGA resources. The target clock frequency should be 50 MHz.

Tasks

Perform the following tasks:

1. Write a VHDL code of the execution unit of the described above circuit (shown in the block diagram above).
2. Write a testbench verifying the operation of your execution unit.
3. Perform functional simulation of your circuit and use it to debug your VHDL code.
4. Design a control unit of your circuit. If you do not know how to do it, go to Step 6.
5. Write a testbench verifying the operation of your entire code.
6. Synthesize your circuit using Synplify Pro. Save the RTL schematic.
7. Implement your circuit using Xilinx ISE.
8. Perform timing simulations of your circuit using Active-HDL.
9. Run the static timing analysis of your circuit.
10. Based on the circuit block diagram and the implementation reports, determine the most critical path in your circuit and its length.

Deliverables

1. VHDL code of your entire circuit fulfilling the requirements specified in the Design Requirements section above (source code files)
2. VHDL code of your testbenches (source code file)
3. RTL schematic of your circuit (screenshot)
4. Timing waveforms from the functional simulation demonstrating the correct operation of your circuit (waveform format file)
5. Description of the critical path in your circuit
6. Timing waveforms from the timing simulation demonstrating the delay of the circuit most critical path (waveform format file)
7. FPGA resource utilization
8. Minimum clock period of your circuit.