# Midterm Exam

# ECE 448
# Spring 2010

# Thursday Section

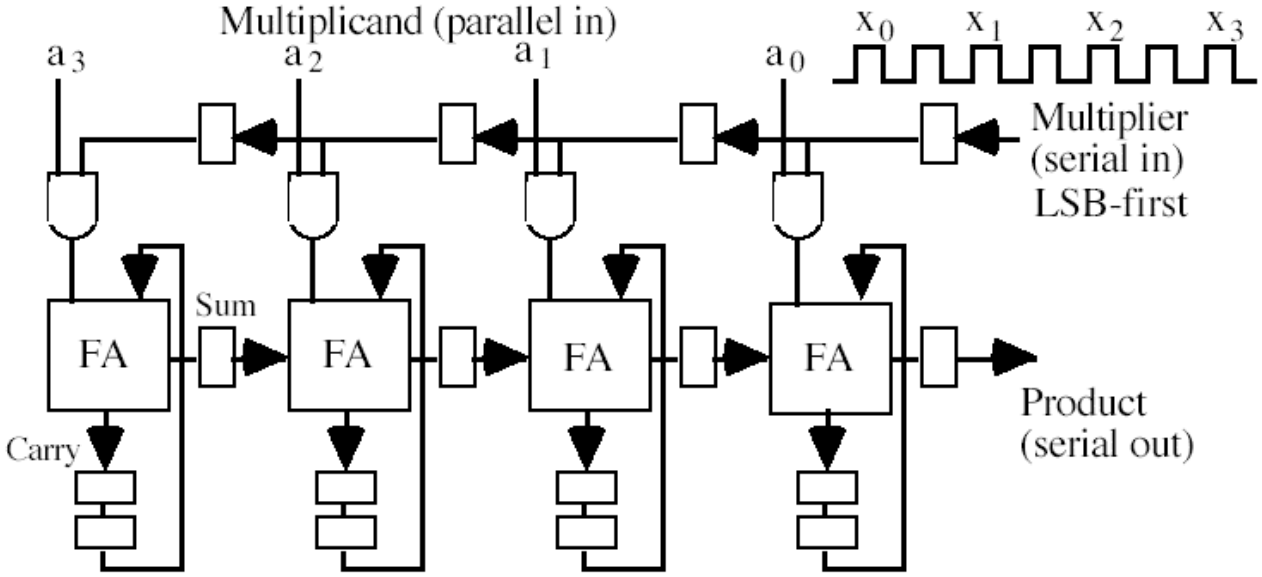
# (15 points)

**Instructions**
Zip all your deliverables into an archive <last_name>.zip and submit it through Blackboard no later than Thursday, March 18, 10:15 PM EST.

**Introduction**

Your task is to describe in VHDL, debug, and implement a digital circuit called Systolic Bit-Serial Multiplier, a special kind of an unsigned integer multiplier, optimized for minimum area, maximum clock frequency, and regular structure. This circuit multiplies two unsigned k-bit numbers, `a` and `x`, and generates as a result `Product` = `a` · `x`.

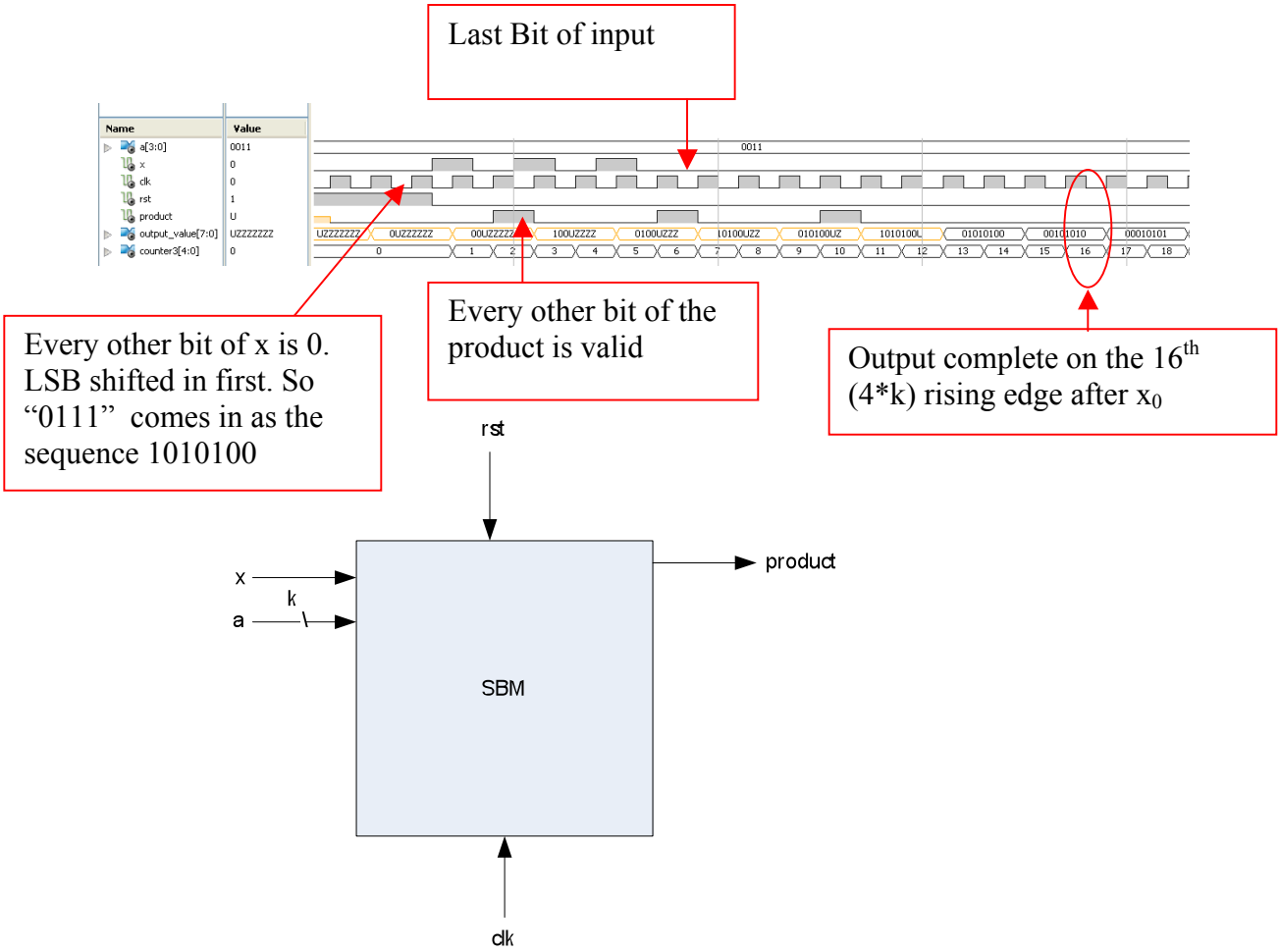
Bellow is a block Diagram of a Systolic Bit-Serial Multiplier for k=4. The small rectangles in this diagram represent D flip-flops. Each flip-flop is assumed to have the reset and clk inputs, not shown in the diagram.




The multiplicand `a` is provided using a parallel input, and the multiplier `x`, is provided using a serial input, with least significant bit (LSB) entering first. Because the caries are delayed by two clock cycles, every valid bit of `x` coming in must be followed by a zero. Also only every other bit of the serial output `Product` is valid. The `Product` comes out in LSB first order, for the 4k clock cycles.

Your task is to either
describe this circuit first for the case of k=4, and then generalize it for the case of an arbitrary integer value of k>1,
or describe it from the beginning in the general form, with an arbitrary input size k>1.

Example Waveform
x=7 (0111) a=3(0011) product = 21(00010101)




| Port name | Mode | Bits | Description |
|---|---|---|---|
| clk | in | 1 | 50 MHz clock with 50% duty cycle |
| reset | in | 1 | Active high synchronous reset |
| a | in | k | The parallel multiplicand |
| x | in | 1 | Serial input multiplicand (LSB first; every other bit is zero) |
| product | out | 1 | Serial output (LSB first; every other bit is valid) |

**Design Requirements**

The combinational portion of the circuit should be described using the dataflow VHDL code, and the sequential portion of the circuit should be described using the synthesizable behavioral code. Your code should infer a circuit that requires a minimum amount of FPGA resources. The target clock frequency should be 100 MHz.

**Tasks**

Perform the following tasks:

1. Write a synthesizable VHDL code representing the described above circuit for the generic value of k. If you do not know how to do it, write the code specifically for k=4.
2. Write a testbench verifying the operation of your circuit for the case of k=4, x=7, and a=3, and at least one more pair of values (a, x).
3. Perform functional simulation of your circuit and use it to debug your VHDL code. Save the obtained timing waveforms.
4. Synthesize your circuit for the case of k=4. Save the obtained RTL schematic.
5. Perform post-synthesis simulations of your circuit. Save the obtained timing waveforms.
6. Implement your circuit using
   FPGA family: Spartan3E,
   Device: 3s100cp132
   Speed Grade: -4.
7. Run the static timing analysis of your circuit.
8. Based on the circuit block diagram and the implementation reports, determine the most critical path in your circuit and the circuit maximum clock frequency.
9. Based on the implementation reports and the report from the static timing analysis, determine the number of CLB slices, Logic Cells, LUTs, D flip-flops, and pins used by the circuit.

**Deliverables**

1. VHDL code of your entire circuit fulfilling the requirements specified in the Design Requirements section above.
2. VHDL code of your testbench.
3. RTL schematic of your circuit.
4. Timing waveforms from the functional and post-synthesis simulations demonstrating the correct operation of your circuit.
5. Description of the critical path of your circuit.
6. FPGA resource utilization (as defined in Task 9 above)
7. Minimum clock period and maximum clock frequency of your circuit.