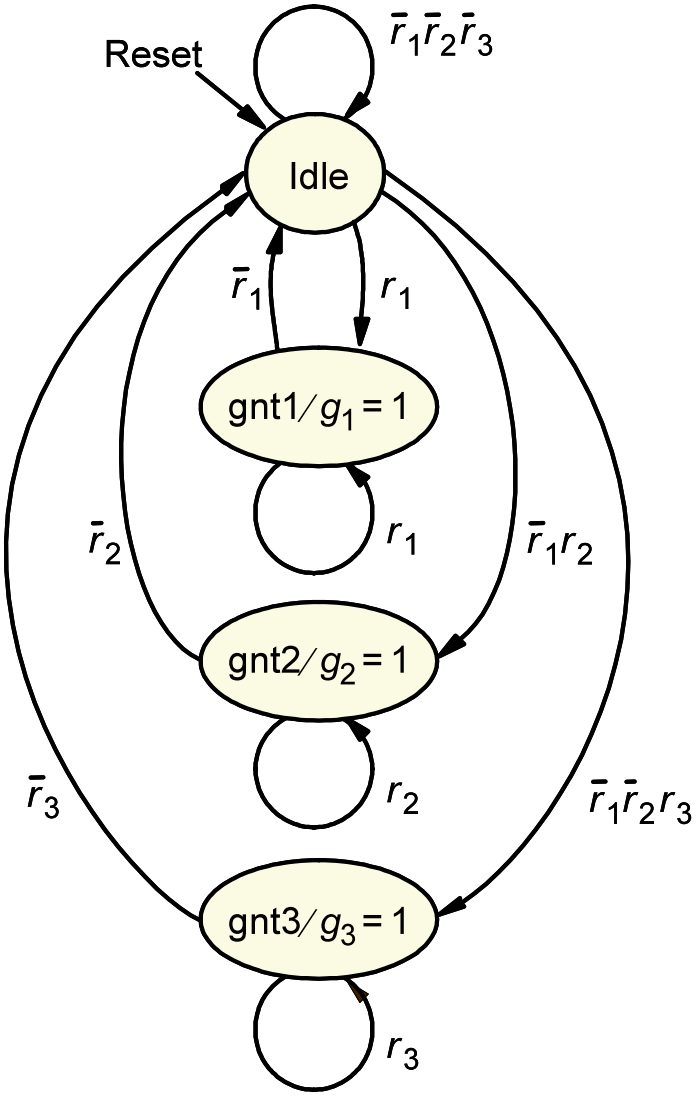
ECE 448
Midterm Exam
Thursday, March 3, 2011

Problem 1 (20%)

Assuming state diagram given below, supplement timing waveforms given in the answer sheet with the correct values of signals **State**, **g1**, **g2**, **g3**, in the interval from 0 to 575 ns.

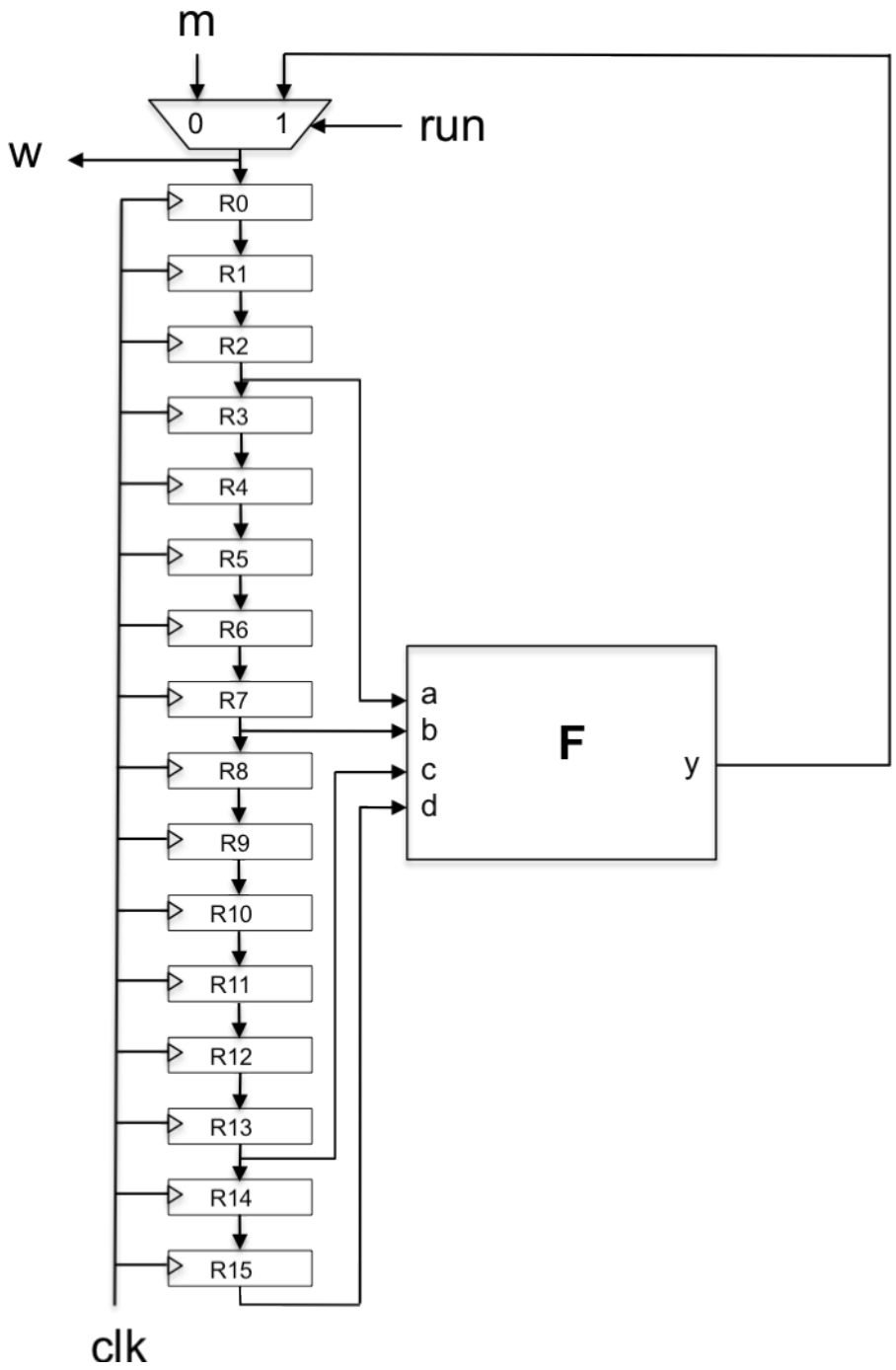


Problem 2

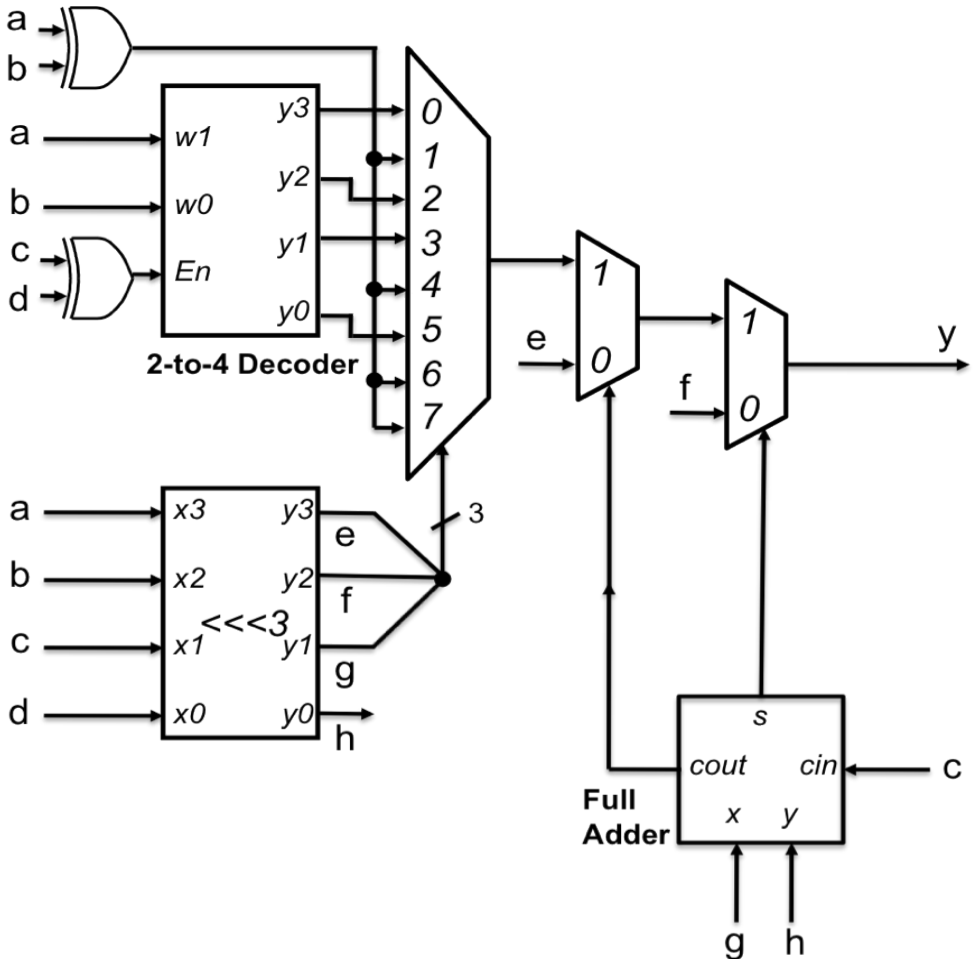
Introduction

The digital circuit shown in the diagrams below is called a Non-linear Feedback Shift Register (NFSR). The Feedback Function F of this circuit is given by the block diagram shown on the next page.

NFSR: Top-Level Circuit



NFSR: Feedback Function F



The meaning of components in the above diagrams is given below:
R0-R15: 1-bit registers (D flip-flops),
<<< k : rotation by k positions to the left.

For the circuit described using the above block diagrams, perform the following tasks:

Task 1 (40% of points)

A. Write entity declaration and architecture of the Top-Level Circuit using **mixed design** style, including: the **dataflow, behavioral, and structural** design styles **Hint: when choosing a design style for a given part of the block diagram, do it in such a way to minimize the total number of lines of VHDL code.**

B. Write entity declaration and architecture of the Feedback Function F, using **exclusively dataflow** design style.

Task 2 (20% of points)

Write a testbench that performs the following tasks:

1. It initializes NFSR with the hexadecimal value P=0x00CE using only inputs shown in the top-level diagram. This initialization should work properly in the circuit after synthesis and implementation. After initialization, R0 should contain the least significant bit of P, and R15 should contain the most significant bit of P.
2. It collects values of the output w, during the first 16 clock cycles after the initialization, in the signal Q of the size of 16 bits. At the end of simulation, Q(0) should contain the first value of w after initialization, Q(1) the second value, …, and Q(15) the 16^{th} value after initialization.

Assume clock signal operating at the frequency of 100 MHz.

Task 3 (20% of points)

Based on your knowledge of the internal structure of Spartan 3E FPGAs, and assuming that NFSR is implemented using CLB slices only, perform the following tasks:

1. In the diagrams provided in the answer sheet, please circle any portion of logic that can be implemented using a **single**:
   - Multipurpose Look-up Table – MLUT,
   - Carry&Control Logic – C&C, or
   - Storage Element – SE.

2. Next to each circle write an abbreviation of an appropriate part of Logic Cell, i.e.,
   - MLUT,
   - C&C, or
   - SE.

3. For pieces of logic implemented using MLUTs, write also, after comma, the corresponding mode of operation,
   - ROM,
   - RAM, or
   - SR (shift register).

   For example, you can write next to a circle:

   SE
   MLUT, ROM
   MLUT, RAM
   C&C.

4. How many logic cells (Logic Cell = ½ of a CLB slice) are needed to implement the entire circuit?

Assume that multiple logic components can be implemented using a single MLUT, but only one part of each Logic Cell (MLUT or **SE** or **C&C) is utilized within each Logic Cell.**