

**ECE 448**  
**Final Exam – Part 1**  
**Spring 2011**

1. Your name:

2. List at least three advantages of FPGAs when compared to ASICs

3. The recent study regarding the comparison of the area, speed, and power of ASICs vs. FPGAs, reported in the paper assigned to you as your required reading, used the following number of representative circuits as examples

- a. about 5
- b. about 15
- c. about 25
- d. about 50
- e. about 100
- f. about 1000

4. An average ratio of the FPGA area to ASIC area for two circuits performing the same function (assuming the use of logic only in FPGAs) is equal to approximately:

- a. 2      b. 3      c. 10      d. 20      e. 30      f. 40      g. 50

5. How many words of the size of 32 bits can be held in a single Block RAM in Spartan 3E FPGA?

How many parity bits can accompany each data word?

6. What is the name (including the number) of the two most recent families of Altera FPGA devices in each of the following categories:

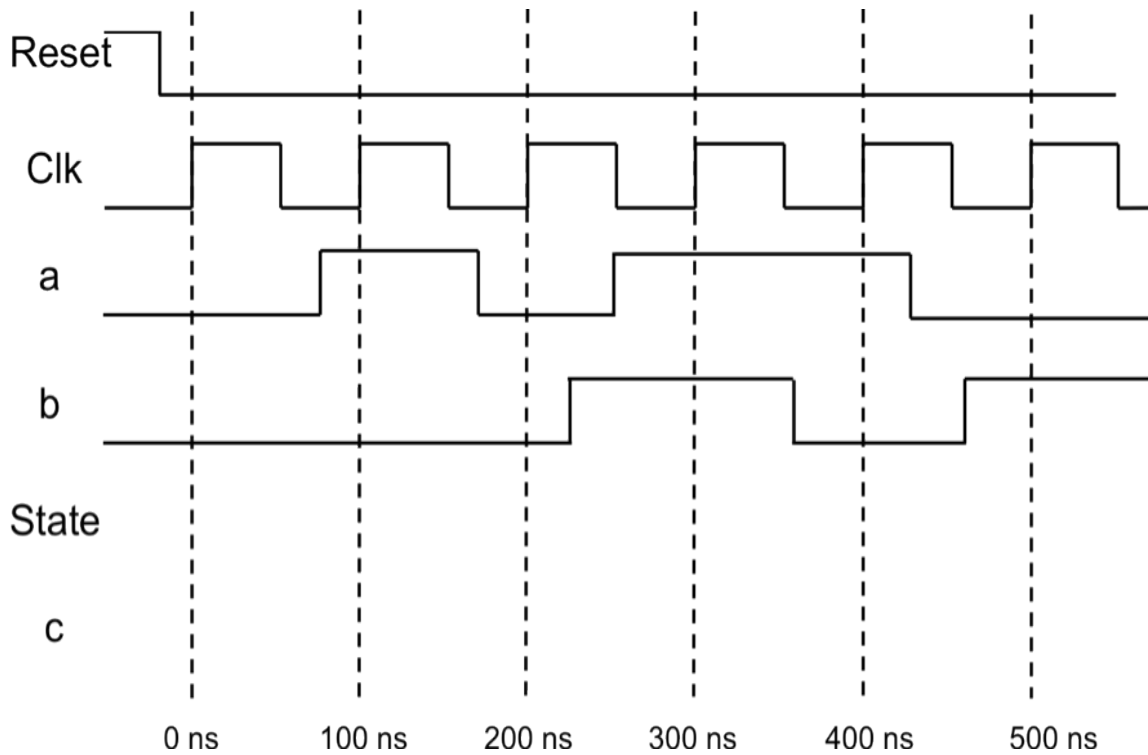
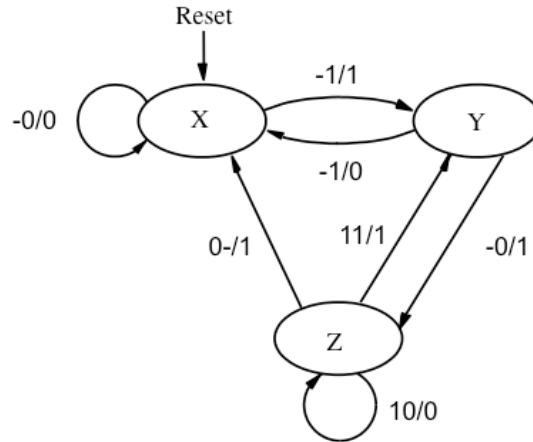
low-cost:

mid-range:

high-performance:

7. What is the name of the hardwired microprocessor embedded in selected Xilinx high performance FPGAs?

8. Assuming the state diagram given below, supplement timing waveforms given in the answer sheet with the correct values of the internal state **State** and the output **c**, in the interval from 0 to 575 ns.



**9. Based on your knowledge of the internal structure of Spartan 3E FPGAs, and assuming that the following circuit is implemented using CLB slices only, perform the following tasks:**

a. In the diagrams provided in the answer sheet, please circle any portion of logic that can be implemented using a **single**:

- Multipurpose Look-up Table – MLUT,
- Carry & Control Logic – C&C, or
- Storage Element – SE.

b. Next to each circle write an abbreviation of an appropriate part of Logic Cell, i.e.,

- MLUT,
- C&C, or
- SE

c. For pieces of logic implemented using MLUTs, write also, after comma, the corresponding mode of operation,

- ROM,
- RAM, or
- SR (shift register).

For example, you can write next to a circle: SE MLUT, ROM MLUT, RAM C&C.

d. How many logic cells (Logic Cell = 1/2 of a CLB slice) are needed to implement the entire circuit?

**Assume that multiple logic components can be implemented using a single MLUT, but only one part of each Logic Cell (MLUT or SE or C&C) is utilized within each Logic Cell.**

