# Midterm Exam

# ECE 448
# Spring 2011

# Monday Section
# (15 points)

**Instructions:**
Zip all your deliverables into an archive <last_name>.zip and submit it through Blackboard no later than Monday, March 7, 10:15 PM EST.

**Introduction:**
Design a Moving-Average Persistent-Peak Detector (MA-PPD) circuit. The purpose of the MA-PPD is to alert the user when samples of a signal persist too long beyond a threshold. The circuit consists of a moving average calculation, a peak detector circuit, and counters to keep track of the length of time a signal stays beyond the threshold.

The user provides:
- a stream of signed input samples (x, with bit width M)
- the log2 of the averaging length (avg_len)
- threshold value (threshold)
- persistence length (persist_len)

The circuit outputs a 1-bit signal to alert the user.

**Pseudocode:**

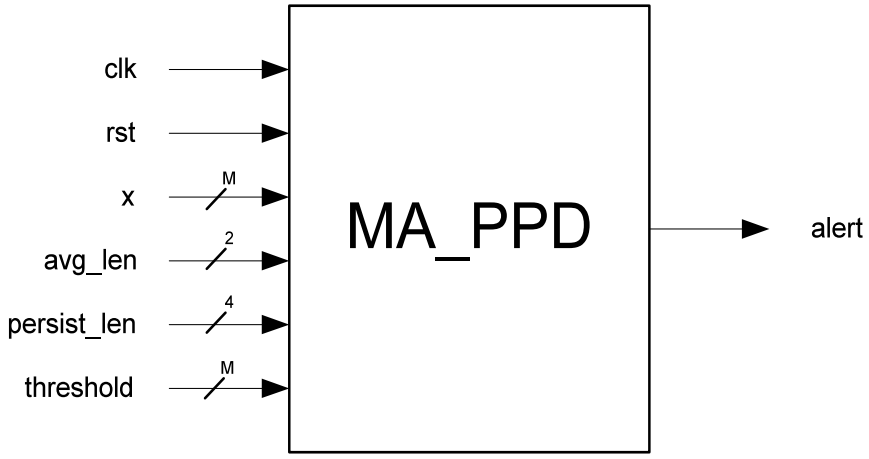
```
sum = 0
loop
   sum = sum + x(i) - x(i-(2^avg_len))
   avg = sum/(2^avg_len)

   if avg>=0 and avg>threshold
       if persist_pos<15
            persist_pos++
       end if
   else
       if persist_pos>0
            persist_pos—
       end if
   end if

   if avg<0 and abs(avg)>threshold
       if persist_neg<15
            persist_neg++
       end if
   else
       if persist_neg>0
            persist_neg—
       end if
   end if

   if persist_pos>persist_len or persist_neg>persist_len
      alert = 1
   else
      alert = 0
   end if
```

**Input sample notation:**
The port for the input samples is labeled x. x(i) represents the current sample. x(i-1) represents the last sample. x(i-2) represents the sample before x(i-1). Etc.

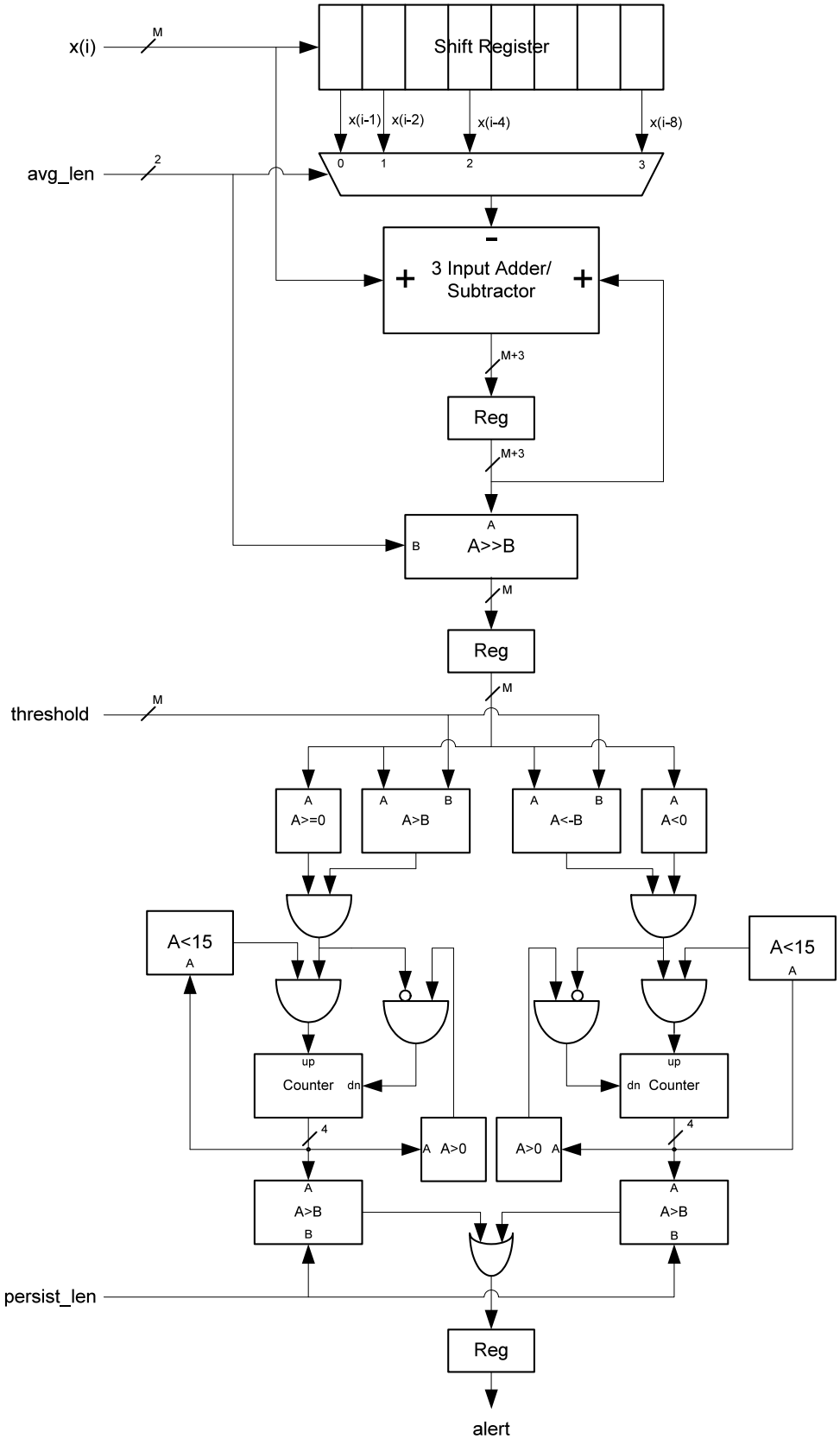
**Range of Values:**
x range is –2^(M-1) to +2^(M-1)-1
avg_len range is 0 to 3
- avg_len = 0 signifies an averaging length of 1
- avg_len = 1 signifies an averaging length of 2
- avg_len = 2 signifies an averaging length of 4
- avg_len = 3 signifies an averaging length of 8

threshold range is 0 to 2^(M-1)-1
persist_len range is 0 to 14

**Ports and Generics:**
Use the labels in the following diagram for you port names. M is generic.



**Circuit Diagram:**
Use the VHDL array construct to generate the shift-register.



## Design Requirements:

Code the entire MA-PPD design using RTL VHDL code. Your code should infer a circuit that requires a minimum amount of FPGA resources. The target clock frequency should be 100 MHz.

## Tasks:

Perform the following tasks:

1. Write a synthesizable VHDL code representing the described above circuit.
2. Write a test bench verifying the operation of your circuit for the case of:
    - M = 8
    - avg_len = 1
    - persist_len = 2
    - threshold = 50

Use the provided package file containing the input vectors to test your circuit.

3. Perform functional simulation of your circuit and use it to debug your VHDL code. Save the obtained timing waveforms.
4. Synthesize your circuit for the case of M=8.
5. Implement your circuit using
    - FPGA family: Spartan3E,
    - Device: 3s100cp132
    - Speed Grade: -4.
6. Run the static timing analysis of your circuit.
7. Based on the circuit block diagram and the implementation reports, determine the most critical path in your circuit and the circuit maximum clock frequency.
8. Based on the implementation reports and the report from the static timing analysis, determine the number:
    - CLB slices
    - Logic Cells
    - LUTs
    - D flip-flops
    - pins
9. Using the same configuration as in Task2, perform timing simulation at the maximum clock frequency identified using static timing analysis. Save the obtained timing waveforms.

## Deliverables:

1. VHDL code of your entire circuit fulfilling the requirements specified in the Design Requirements section above.
2. VHDL code of your test bench.
3. Timing waveforms from the functional and timing simulations demonstrating the correct operation of your circuit.
4. Description of the critical path of your circuit.
5. FPGA resource utilization (as defined in Task 9 above)
6. Minimum clock period and maximum clock frequency of your circuit.