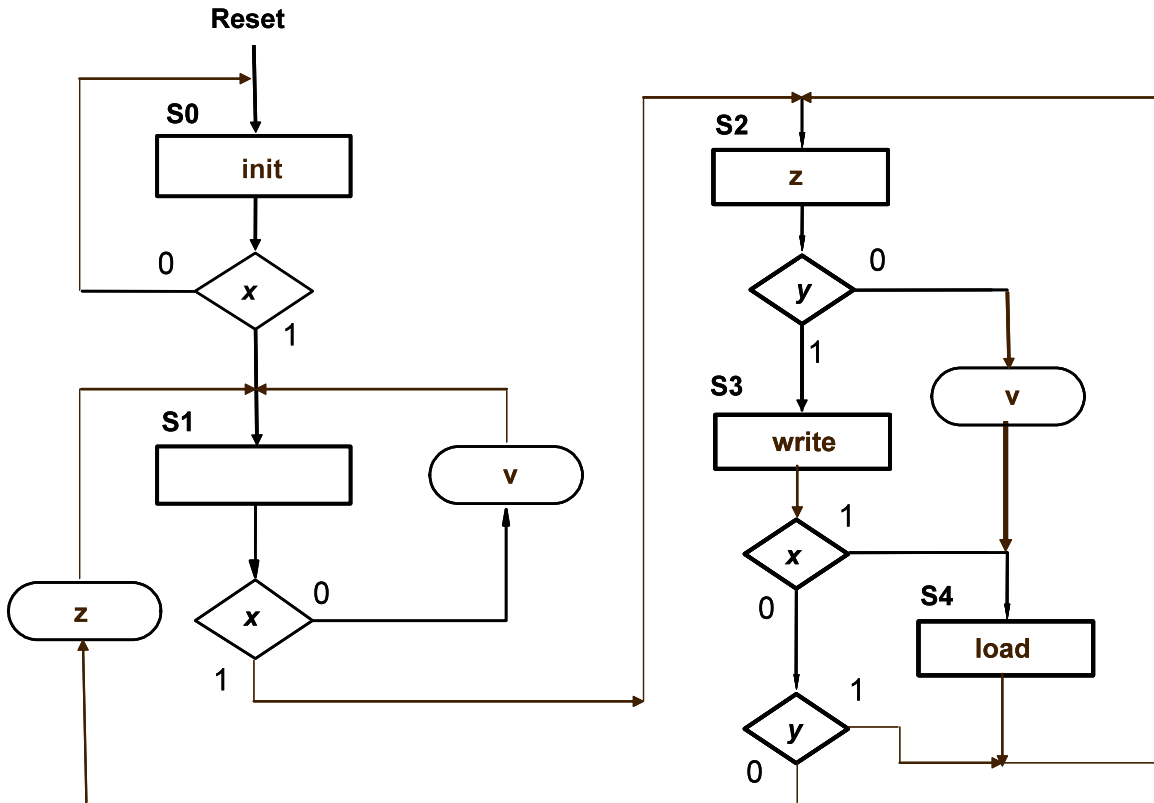


ECE 448
Midterm Exam
Thursday, March 1, 2012

Problem 1 (20%)

Assuming the controller described using the given below ASM chart, supplement timing waveforms provided in the answer sheet with the values of the state s and the values of all outputs from the controller.



Problem 2 (20%)

Draw a block diagram of a digital circuit with the following interface and functionality:

Interface:

Din – 16-bit data input

Dout – 16-bit data output

Addr – 3-bit address of the location (register) where input data is stored and output data is read from

Read – control signal indicating read

Write – control signal indicating write

Clk – clock

Functionality:

If Write = 1, then at the next rising edge of the clock, data from the input Din is stored in the internal location given by the address Addr.

If Read = 1, data from the location given by the address Addr is transferred to the output Dout, and the contents of the internal memory (registers) does not change. If Read=0, the output Dout should be set to the high impedance state.

Assume that the internal memory is implemented using registers. Use only medium scale components, such as registers, multiplexers, encoders, decoders, buffers, etc.

You are not allowed to use RAM in your circuit.

Problem 3 (20%)

For the circuit given below, determine how many Logic Cells are necessary to implement each major component of this circuit, i.e.,

- a) registers R0, R1, R2, R3
- b) adder
- c) subtractor
- d) comparator.

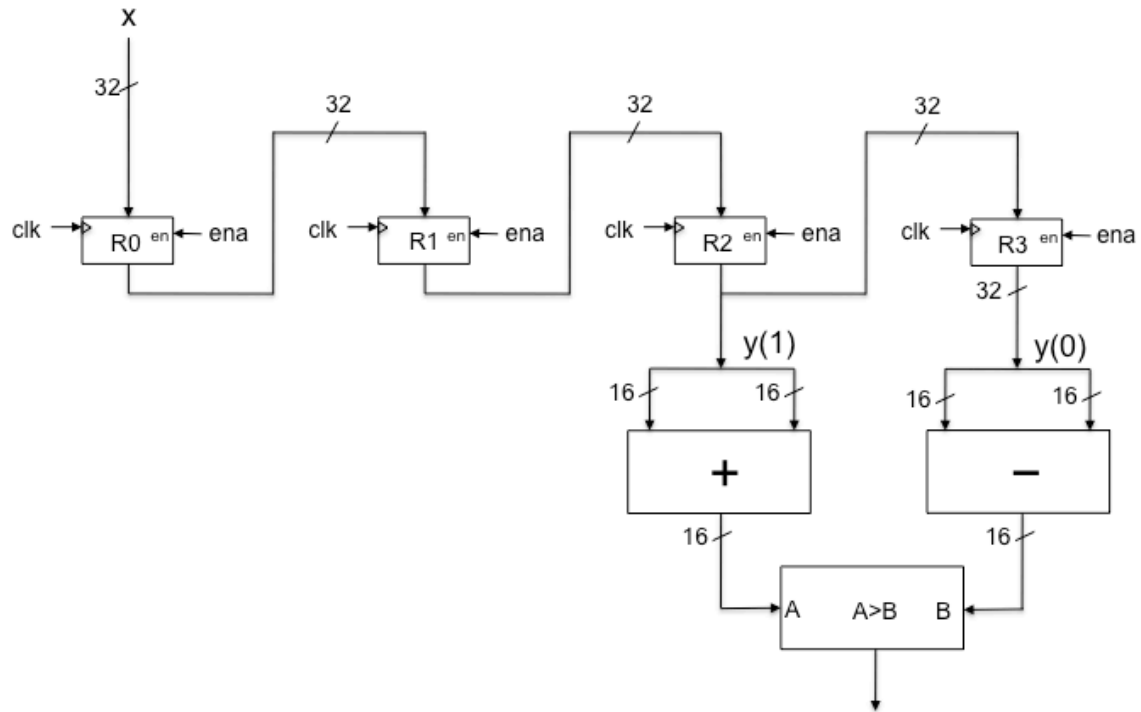
For each major component, describe which parts of a Logic Cell are used for its implementation:

- Multipurpose Look-up Table – MLUT,
- Carry&Control Logic – C&C, or
- Storage Element – SE?

For the pieces of logic implemented using MLUTs, write also, after comma, the corresponding mode of operation,

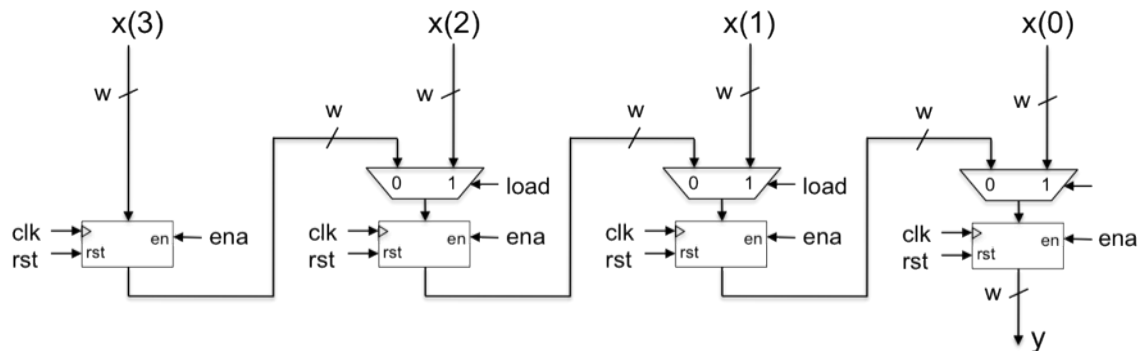
- ROM (logic),
- RAM, or
- SR (shift register).

How many logic cells (Logic Cell = $\frac{1}{2}$ of a CLB slice) total are needed to implement the entire circuit?



Problem 4 (40%)

The digital circuit shown in the diagrams below is called a PISO (Parallel-In-Serial-Out) unit.



Perform the following tasks for this circuit:

- Write entity declaration and architecture, with the size of the output bus, w , treated as a generic with the default value equal to 8.
- Show how to instantiate this component with the value of $w=32$, the input x connected to the signal A : `std_logic_vector(127 downto 0)`, and the output y connected to the signal C : `std_logic_vector(31 downto 0)`.