

**ECE 448
Final Exam – Part I
Spring 2012**

Your name:

1. (1 point) How many words of the size of 8 bits can be held in a single Block RAM in Spartan 3E FPGA?

How many parity bits can accompany each data word?

2. (0.5 point) An approximate number of CLB slices necessary to implement PicoBlaze in Spartan 3 FPGAs is equal to:

- a) 50 b) 100 c) 500 d) 1000 e) 5000

3. (0.5 point) What is the name of the hardwired microcontroller implemented in the most recent family of Xilinx FPGAs, called Zynq

4. (1 point) Show how to implement Full Adder using a single 2-to-1 multiplexer, and a minimum number of logic gates. Hint: You can use the way the Full Adder is implemented in Xilinx FPGAs.

5. (2 points) What is a minimum number of Spartan 3 Logic Cells (one Logic Cell = $\frac{1}{2}$ of a CLB Slice) necessary to implement

- a. Functions $y_1 = x_1x_2 + x_2x_3 + x_1x_3x_4x_5$, $y_2 = x_1x_2 + x_4 + x_5$
- b. 32-bit unsigned comparator ($A > B$)
- c. 48-bit shift register with serial input, serial output, and enable
- d. 48-bit shift register with serial input, serial output, and reset
- e. 32x8 dual-port RAM

Which components of Logic Cells (Multipurpose LUT, Carry & Control, Storage Element) are used in each case, and in which mode of operation (ROM, RAM, shift-register, fast carry logic, latch, flip-flop, etc.) they work?