ECE 448
Final Exam – Part 1
Spring 2012

1. Your name:

2. List at least three advantages of ASICs when compared to FPGAs

3. The recent study regarding the comparison of the area, speed, and power of ASICs vs. FPGAs, reported in the paper assigned to you as your required reading, was performed at

a. MIT
b. GMU
c. GWU
d. University of Toronto
e. Carnegie Melon University
f. UCLA
g. Stanford

4. An average ratio of the ASIC speed vs. the speed of a fastest grade FPGA, for two circuits performing the same function (assuming the use of logic only in FPGAs) is equal to approximately:

a. 0.5 b. 1 c. 2 d. 3 e. 5 f. 10 g. 20 h. 30

5. How many words of the size of 16 bits can be held in a single Block RAM in Spartan 3E FPGA?

How many parity bits can accompany each data word?

6. What is the name (including the number) of the two most recent families of Xilinx FPGA devices in each of the following categories:

low-cost:

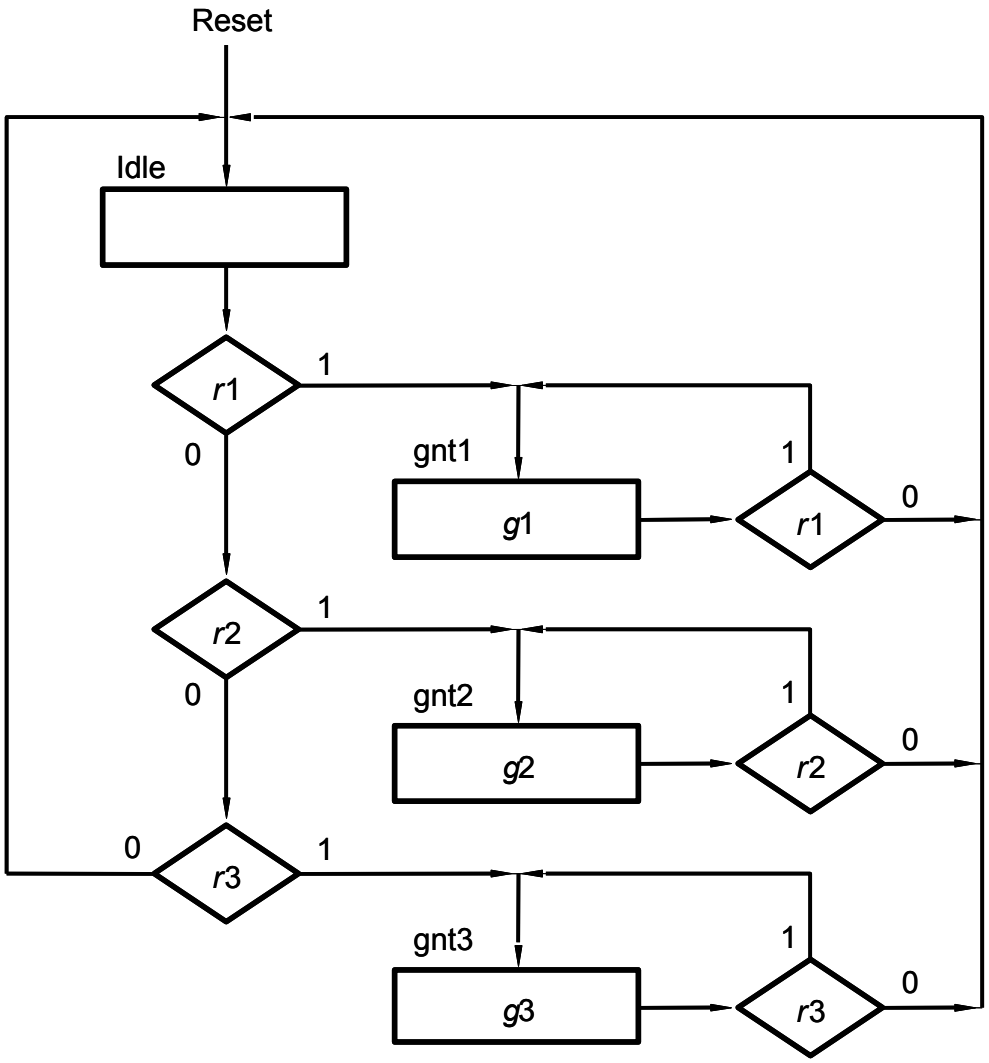
mid-range:

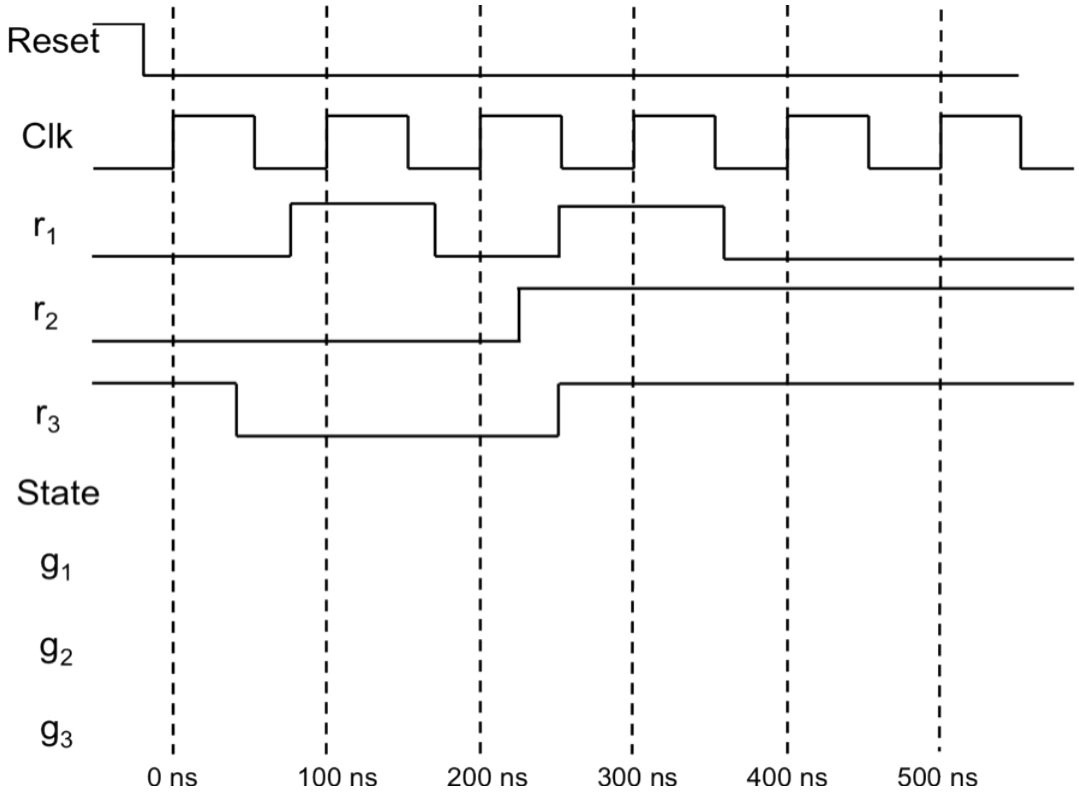
high-performance:

7. The carry & control logic used in Spartan 3E FPGAs to implement fast addition is aimed primarily at minimizing the following delay of a Full Adder (assuming the Full Adder has inputs x, y, cin and outputs s, cout).

a) from x, y to cout, b) from cin to cout, c) from cin to s

8. Assuming ASM chart given below, supplement timing waveforms given in the answer sheet with the correct values of signals State, g1, g2, g3, in the interval from 0 to 575 ns.





9. **Based on your knowledge of the internal structure of Spartan 3E FPGAs, and assuming that the following circuits are implemented using CLB slices and routing resources only, perform the following tasks:**

a. In the diagrams provided in the answer sheet, please circle any portion of logic that can be implemented using a **single**:

- Multipurpose Look-up Table – MLUT,
- Carry & Control Logic – C&C, or
- Storage Element – SE.

If given function can be implemented using routing resources only, write ROUTING.

b. Next to each circle write an abbreviation of an appropriate part of Logic Cell, i.e.,

- MLUT,
- C&C, or
- SE

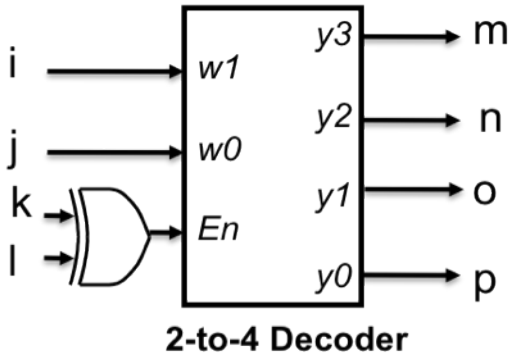
c. For pieces of logic implemented using MLUTs, write also, after comma, the corresponding mode of operation,

- ROM,
- RAM, or
- SR (shift register).

For example, you can write next to a circle: SE MLUT, ROM MLUT, RAM C&C.

d. How many logic cells (Logic Cell = 1⁄2 of a CLB slice) are needed to implement the entire circuit?

Assume that multiple logic components can be implemented using a single MLUT, but only one part of each Logic Cell (MLUT or **SE** or **C&C) is utilized within each Logic Cell.**



2-to-4 Decoder