ECE 448
Midterm Exam
Monday, March 4, 2013

Problem 1 (20%)

Assuming the controller, described using the given below ASM chart:

- supplement timing waveforms provided in the answer sheet with the values of the **state S**, and the values of the **outputs p**, **r**, and **y**
- write the VHDL dataflow code for the output function, calculating **p**, **r**, and **y**.

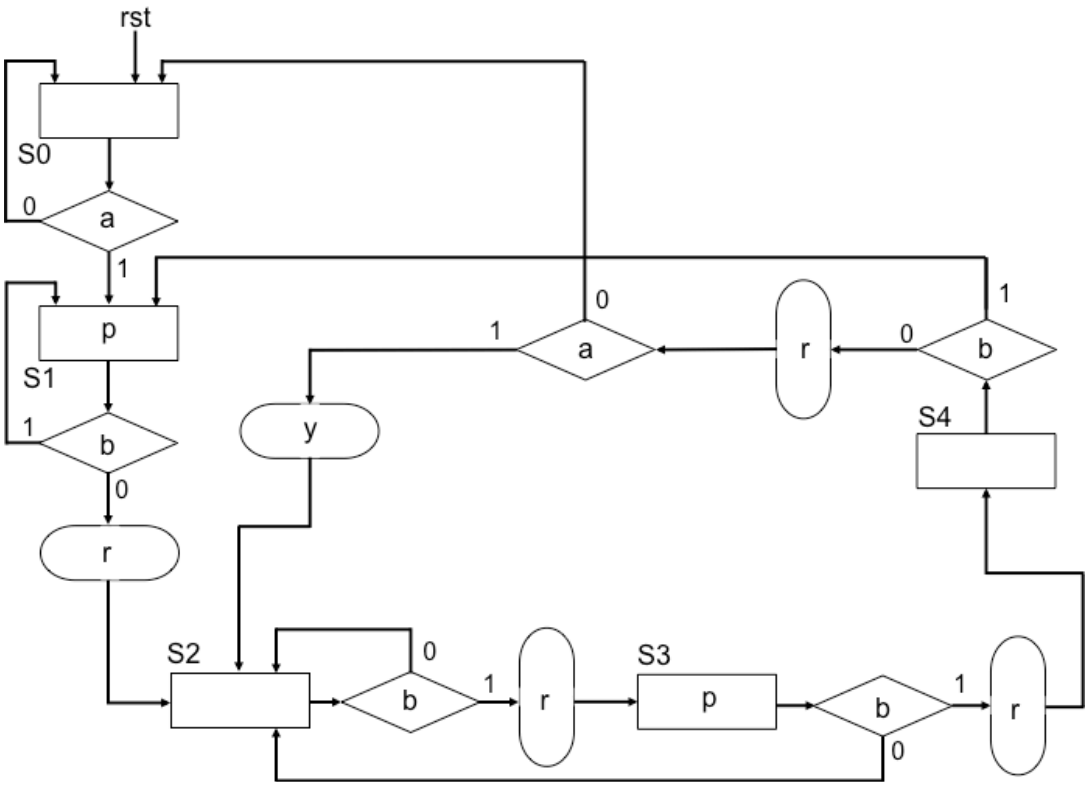

Fig. 1 ASM chart of the controller.

Problem 2 (20%)

Draw a block diagram of the combinational circuit described using the following pseudocode:

Inputs:

A: 8-bit unsigned integer
Sel: 2-bit select signal
En: 1 bit enable input (active low)

Outputs:

X: 4 bit unsigned integer

Intermediate Variables:

Q, R, F, G, J, Xp: 4 bit unsigned integers

E: 1 bit signal

Algorithm:

```
Q = A / 16
R = A  mod 16

if Q is prime then
   F = Q
elsif R is odd then
   F = R
elsif  Q > R
   F = Q / 2
else
   F = R >>> 2
endif

if F ≥ 8 then
   G = 3
elsif F ≥ 4 then
   G = 2
elsif F ≥ 2 then
   G = 1
else
   G = 0.
endif

if F = 0 then
   E = 0
else
   E = 1
end if

if E = 0 then
   J = 0
elsif G = 3
   J = 8
elsif G = 2
   J = 4
elsif G = 1
   J = 2
else
   J = 1
endif
```

```
if Sel = 0 then
   Xp = F
elsif Sel = 1 then
   Xp = G
elsif Sel = 2
   Xp = J
elseif Sel = 3
   Xp = Q+R mod 16
endif

if En = 0 then
   X = Xp
else
   X = "ZZZZ"  -- high impedance state
endif
```

Requirements:

1. You are allowed to use only standard combinational logic components discussed in Lecture 3: Combinational-Circuit Building Blocks. Data Flow Modeling of Combinational Logic.
2. You are not allowed to use a divisor circuit "/", implementing division for an arbitrary value of a divisor. All divisions by powers of two should be implemented using appropriate logic or arithmetic shifts, or bit selection.
3. You are not allowed to use "mod" operator. Replace it by an appropriate bit selection.
4. Clearly mark the widths and directions of all buses in your circuit.
5. You can use connections by name, especially if drawing wires would reduce the readability of your diagram.
6. You can use at most two levels of hierarchy.
7. **<u>In case of using ROM, clearly specify the number of address and data bits. In a separate diagram, please show the memory map (the contents) of your ROM.</u>**

Problem 3 (15%)

Fill in the blanks in the code of MISR (Multiple Input Signature Register), **<u>provided in the answer sheet</u>**. **Do not write this code from scratch**! The block diagram of MISR is shown in Fig. 2.

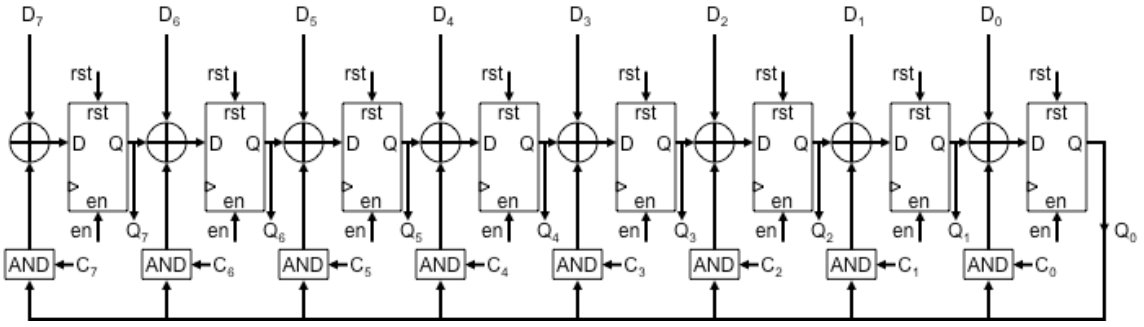

Fig. 2: Block diagram of MISR.

Problem 4 (20%)

Based on your knowledge of the internal structure of the Spartan 6 FPGAs, and assuming that

A. The Debouncer circuit shown in Figs. 3 and 4 is implemented using CLB slices only,

B. Generics k and DD have the following values: k=24, DD = 10,000,000,

perform the following tasks:

1. **In the diagrams provided in the answer sheet**, please circle any portion of logic that can be implemented using:
   - n Multipurpose Look-up Tables – MLUTs, or
   - n Storage Elements – SE,

   where n ≥ 1.

2. Next to each circle write
   - n MLUT, <MLUT_mode>, *or*
   - n SE, <SE_mode>,

   where
   n is the number of the respective FPGA structures (MLUTs or SEs), and
   <MLUT_mode> = ROM (logic), RAM, or SR (shift register),
   <SE_mode> = FF (flip-flop) or LT (latch).

3. For the arithmetic components, implemented using Carry Logic, please circle these components, and write next to them
   n (CL+MLUT),
   where n is the number of the Carry Logic stages used.

Hint: One Carry Logic stage and one associated MLUT can be used to implement one Full Adder.

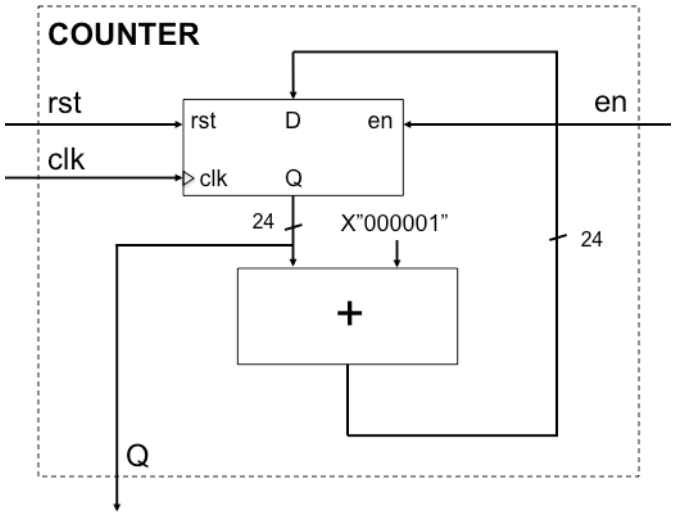

Fig. 3: Implementation of the Counter in the Debouncer circuit.

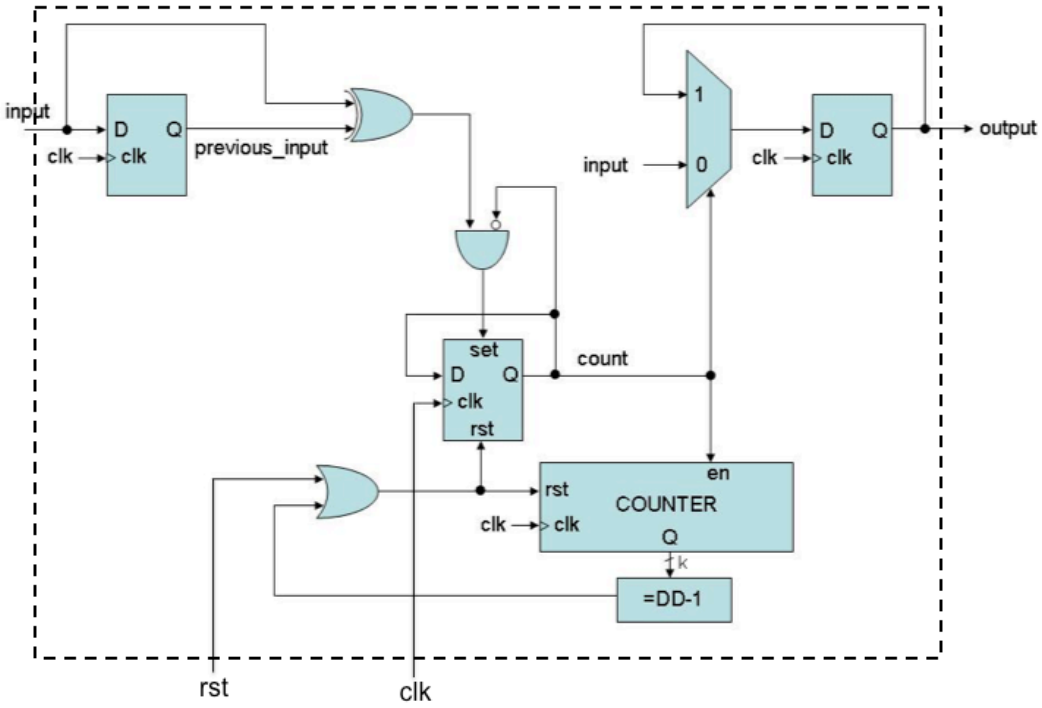

Fig. 4: Block diagram of the Debouncer circuit.

Problem 5 (25%)

Write a complete simple testbench capable of testing the debouncer shown in Fig. 4, by applying

A. clk, B. rst, C. input shown in Fig. 5.

- The clock signal, clk, should be a periodical signal, with the period of 10 ns.
- The reset signal, rst, should be a non-periodical signal, active high for the first 50 ns of the simulation period.
- The input signal should look as shown in Fig. 5, and should have all changes happening on the falling edges of the clock.
- The Debouncer, shown in Fig. 4, should be instantiated with the following values of the generics k and DD: k = 4, DD = 15.

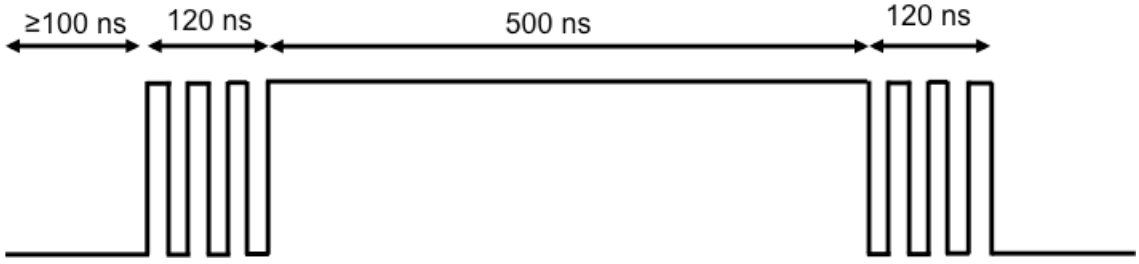

Fig. 5: Timing waveform of the input signal.