Midterm Exam ECE 448

Spring 2013

Thursday Section (15 points)

Instructions:

Zip all your deliverables into an archive <last_name>.zip and submit it through Blackboard no later than Thursday, March 21, 10:15 PM EDT.

Lab Midterm Exam

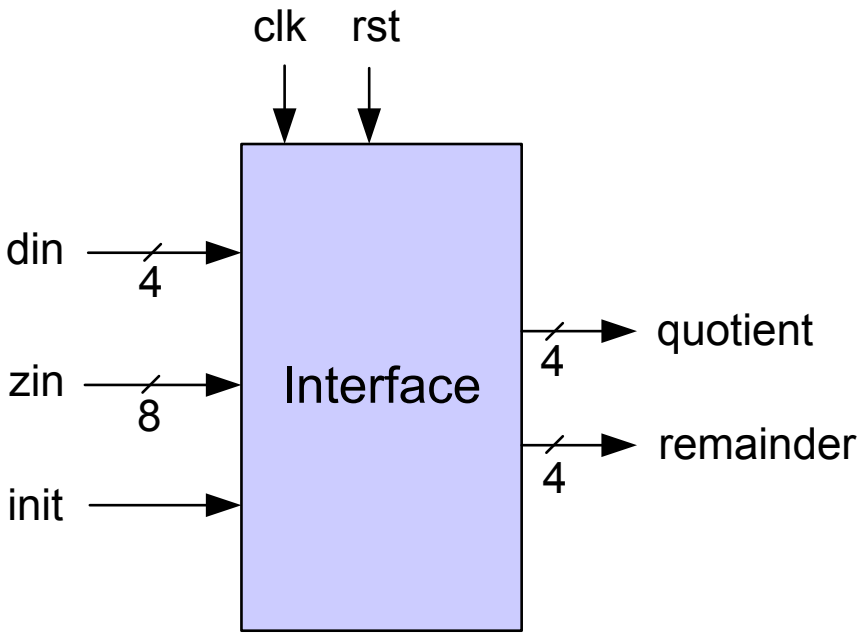
The circuit described below performs the division operation. The design takes an 8-bit unsigned dividend and divides it by a 4-bit unsigned divisor. It produces a 4-bit quotient and a 4-bit remainder as a result. Signal "INIT" is used to initiate the operation.

The circuit is specified below using its:

- Interface
- Table of input/output ports
- Block diagram
- Input/output and waveforms
- Output waveform for functional simulation

Interface:

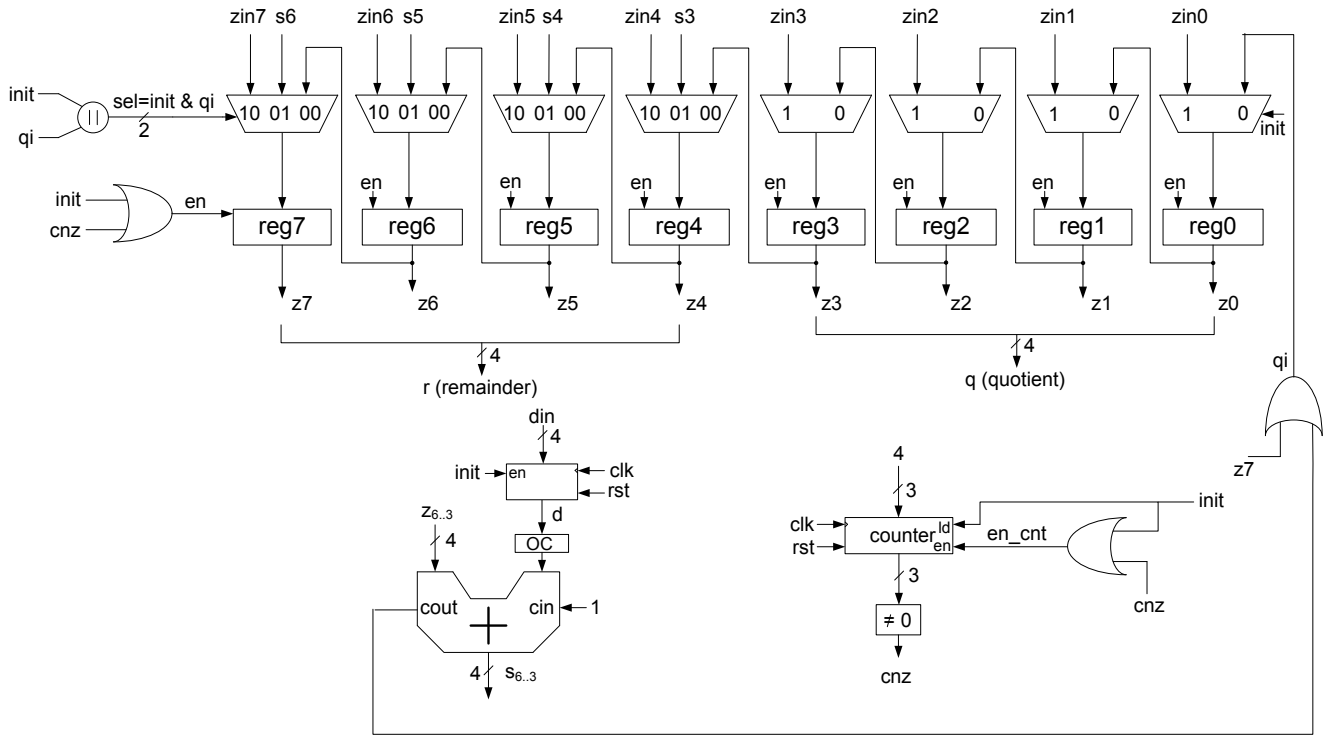
Assume the following interface to your circuit.



Tableofinput/outputports:

Port	Mode	width	Function
clk	IN	1	System clock
rst	IN	1	Asynchronous system reset
din	IN	4	Divisor
zin	IN	8	Dividend
init	IN	1	A signal to initiate division operation
quotient	OUT	4	Quotient
remainder	OUT	4	Remainder

Blockdiagram:



OC denotes one's complement.

Inputs, Outputs and Waveform:

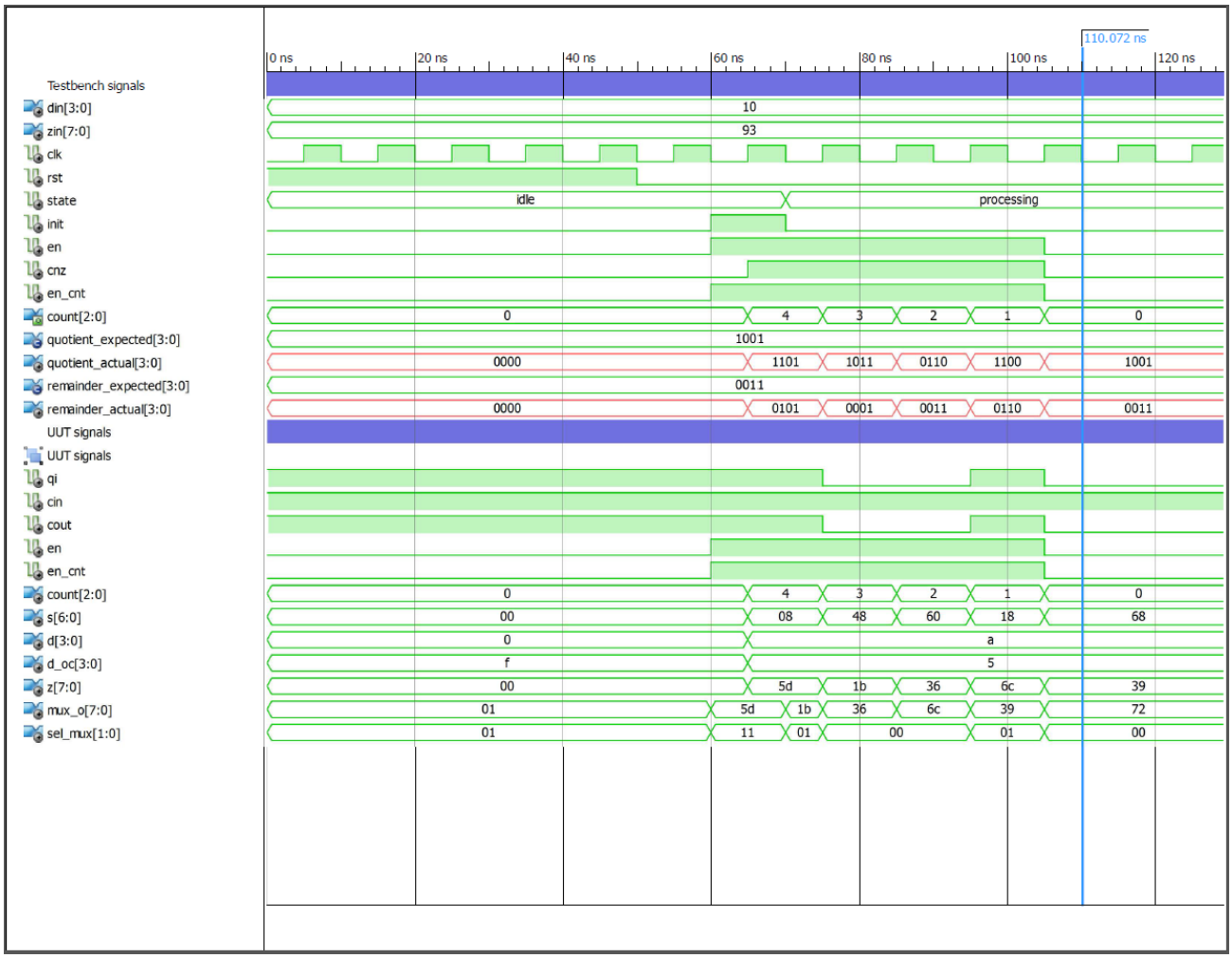
Inputs:

din="1010" = 10
zin="01011101" = 93

Output:

quotient = "1001" = 9
remainder = "0011" = 3

Functional Waveform:



Thursday section

Design Requirements:

The combinational portion of the circuit should be described using the dataflow VHDL code, and the sequential portion of the circuit should be described using the synthesizable behavioral code. Your code should infer a circuit that requires a minimum amount of FPGA resources. The target clock frequency should be **100 MHz**.

Tasks:

Perform the following tasks:

1. Write a synthesizable VHDL code representing the division circuit (shown in the block diagram above).
2. Write a testbench verifying the operation of your division circuit.
3. Perform functional simulation of your circuit and use it to debug your VHDL code. Take a print out of the waveform showing the entire operation using default PDF conversion tool installed in the lab (Use the multiple page option in order to display necessary information on multiple pages, if required).
4. Synthesize your circuit.
5. Implement your circuit using
    a. FPGA family: Spartan 6
    b. Device: xc6slx16-3csg324
    c. Speed Grade: -3
6. Run the static timing analysis of your circuit.
7. Based on the circuit block diagram and the report from the static timing analysis, determine the most critical path in your circuit and the circuit maximum clock frequency.
8. Based on the implementation reports, determine the number of CLB slices, LUTs, flip-flops, and pins used by the circuit.
9. Perform the timing simulation of your circuit at the maximum clock frequency returned by the static timing analysis. Take a printout of the waveform showing the entire operation using default PDF conversion tool installed in the lab (Use the multiple page option in order to display necessary information on multiple pages, if required).

Deliverables:

1. VHDL code of your entire circuit fulfilling the requirements specified in the *Design Requirements* section above.
2. VHDL code of your testbench.
3. Timing waveforms from the functional and timing simulations demonstrating the correct operation of your circuit.
4. Description of the critical path in your circuit
5. FPGA resource utilization (as defined in Task 8 above).
6. Minimum clock period and maximum clock frequency of your circuit.