ECE 448
Midterm Exam
Wednesday, March 5, 2014

Problem 1 (20%)

Assuming the controller described using the given below ASM chart, supplement timing waveforms provided in the answer sheet with the values of the **state S**, and the values of the **outputs p**, **r**, and **y.**

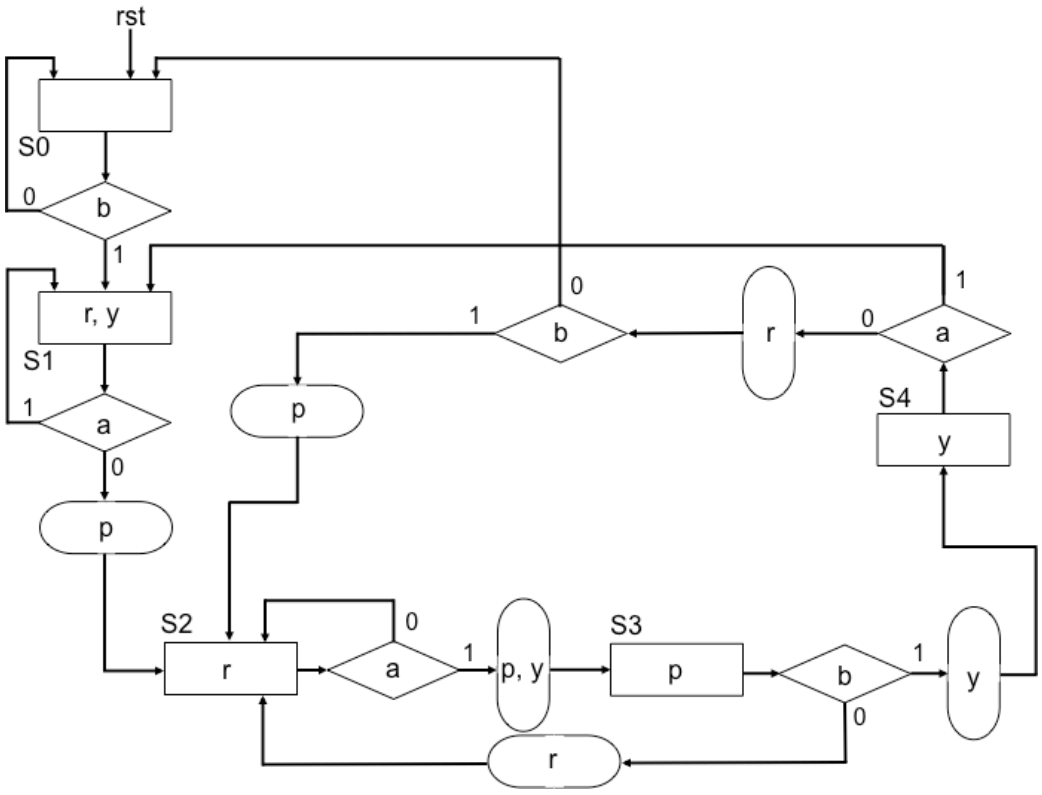

Fig. 1 ASM chart of the controller.

Problem 2 (25%)

Draw block diagrams of

A. 4-to-16 decoder built of 2-to-4 decoders and a minimum number of logic gates
B. 16-to-1 multiplexer built of 4-to-1 multiplexers and a minimum number of logic gates
C. 4-bit priority encoder built of 2-to-1 multiplexers and a minimum number of logic gates (assume that the most significant bit of the input **w** has the highest priority, and the **z** output is equal to 1 when at least one input bit is equal to 1).

For each of the above circuits determine the minimum number LUTs of Spartan 6 FPGAs necessary to implement this circuit. Assume that you can use LUTs belonging to different types of slices (SLICEX, SLICEL, or SLICEM), and the selected type of slice should result in the minimum resource utilization.

Problem 3 (15%)

Fill in the blanks in the code of the Debouncer circuit, **provided in the answer sheet**. **Do not write this code from scratch**! The block diagram of the Debouncer is shown in Fig. 2.

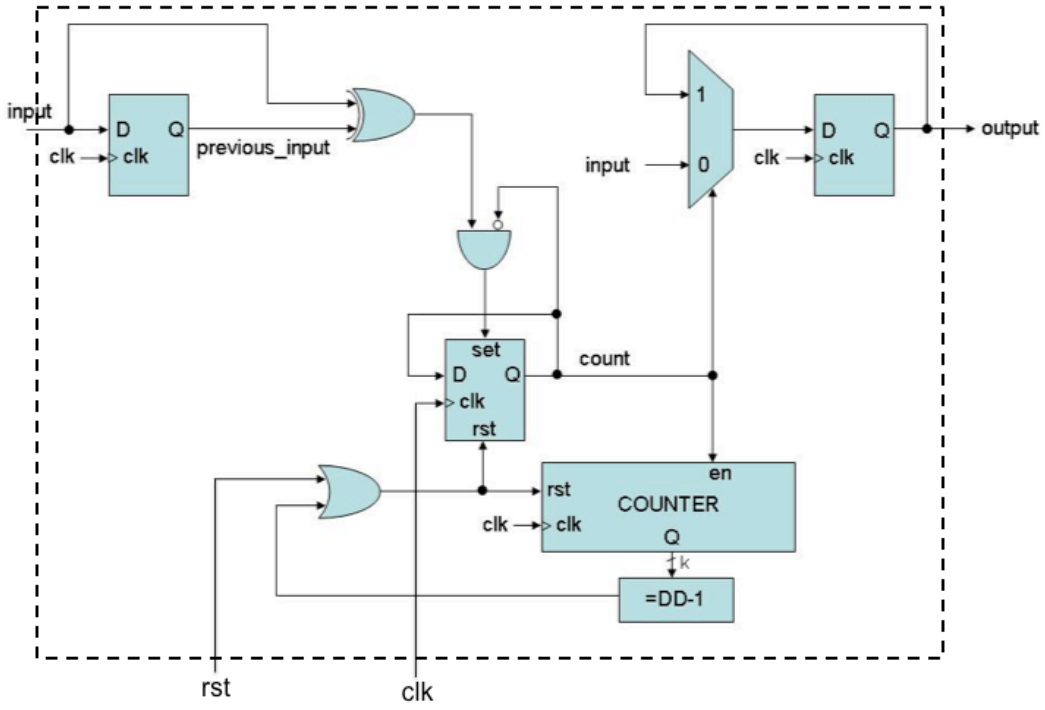

Fig. 2: Block diagram of the Debouncer circuit.

Problem 4 (20%)

Write the VHDL code of the architecture of the circuit called Regular, shown in Fig. 3.

Assume that the signals

m, y, mux_out, R(0), R(1), …, R(15) are 32-bit wide buses.

If you do not know how to solve the problem under this assumption, you can receive a partial credit by writing the code under the assumption that the aforementioned signals are 1-bit wide.

Do your best minimize the length of your code by either using the for-generate statement and/or behavioral VHDL description.

No library, package, or entity declarations are required.

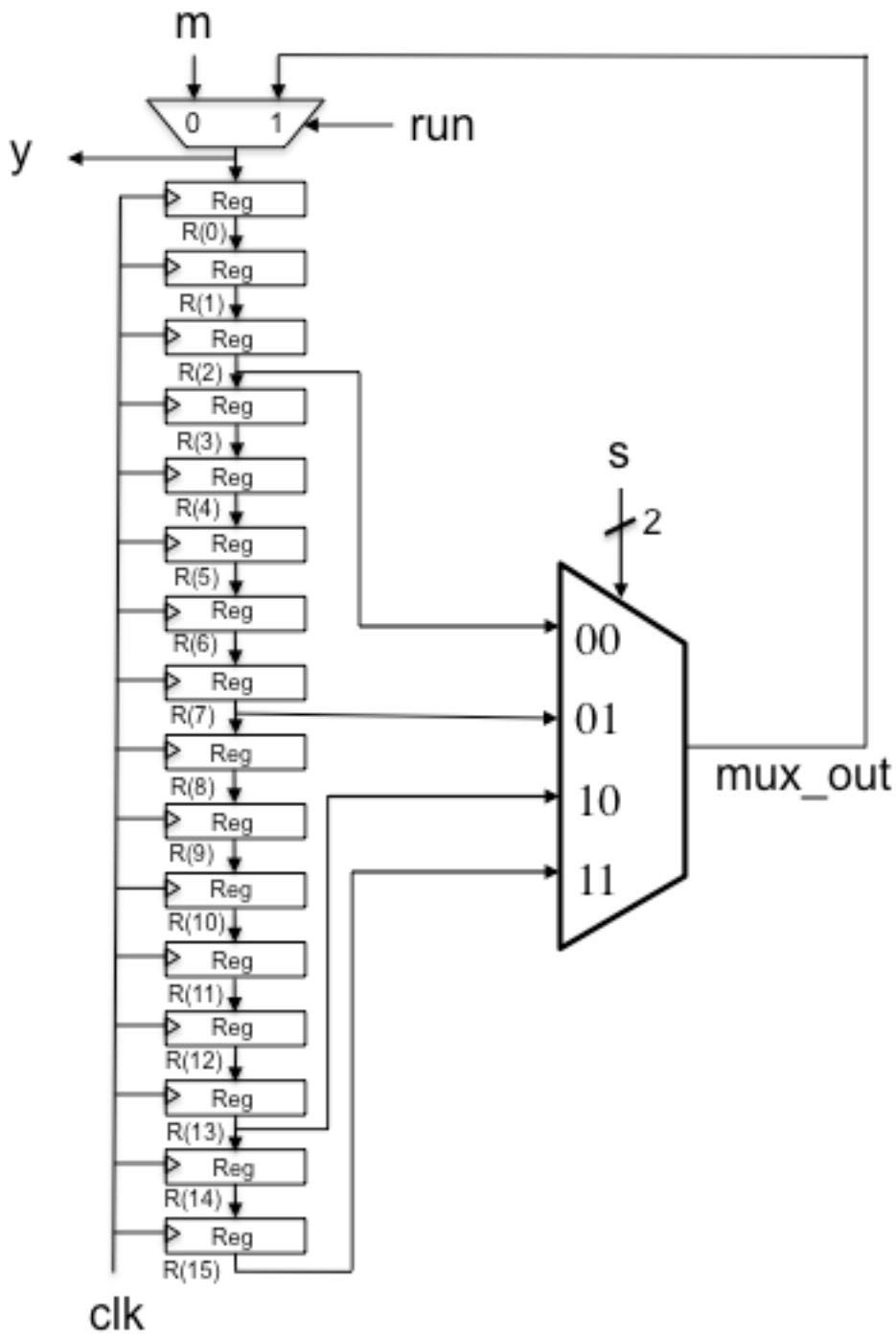

Fig. 3 Block Diagram of the Regular circuit.

Problem 5 (20%)

Write a complete simple testbench capable of generating inputs **rst**, **clk**, **a**, and **b** to the Controller described by the ASM chart shown in Fig. 1, changing according to the timing waveforms shown in Fig. 4.

Assume that the clock signal is periodical, and the remaining signals are non-periodical.

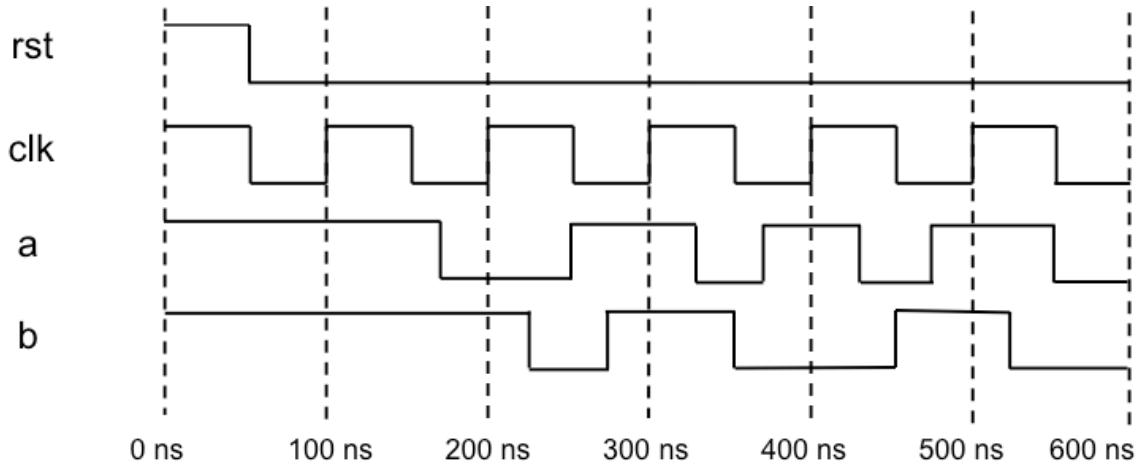

Fig. 4 Timing Waveforms of the Controller Inputs.