ECE 448
Final Exam – Part I
Spring 2014

Your Name:

1. (0.5 point) How many words of the size of 32 bits can be stored in a single Block RAM of a Spartan 6 FPGA?

How many parity bits can accompany each data word?

2. (0.5 point) An approximate number of CLB slices necessary to implement PicoBlaze in Spartan 6 FPGAs is equal to:

a) 25 b) 50 c) 100 d) 250 e) 1000

3. (0.5 point) What is the name of the hardwired microcontroller implemented in the most recent family of Xilinx FPGAs, called Zynq?

4. (0.5 point) An average ratio of the FPGA area to ASIC area for two circuits performing the same function (assuming the use of logic only in FPGAs) is approximately equal to:

a. 2 b. 3 c. 10 d. 20 e. 30 f. 40 g. 50

5. (1 point) What is the minimum <u>number</u> of Spartan 6 LUTs necessary to implement

a. Functions $y_1=x_1x_2+x_2x_3+x_1x_3x_4x_5$, $y_2=x_1x_2+x_4+x_5$
b. 96-bit shift register with serial input, serial output, and enable
c. 64x16 dual-port RAM

<u>Which MLUT mode of operation (ROM, RAM, shift-register) is used in each case?</u>