

Final Exam Spring 2014-Part II

Problem 1 (7.5 points)

Draw a block diagram of the datapath unit of a circuit capable of executing the pseudocode given below.

In this code, MEM_D represents a single-port memory of the size of 2048 x 10. The circuit takes as an input a stream of 8-bit ASCII characters representing a document written in English. It calculates the lengths of 2048 first sentences (i.e., strings ending with '.', '?', or '!') and stores them in MEM_D. Then, it calculates the minimum, maximum, and average length of a sentence in the input text. The document is assumed to contain at least 2048 sentences. All sentences are assumed to be shorter than 1024 characters.

begin:

```
wait for s=1
```

```
done = 0
```

```
i=0; count = 0
```

```
start = 0
```

```
sum=0; max=0; min=1023
```

```
while (count < 2048) do
```

```
  next =din
```

```
  if ((next = '.') or (next = '!') or (next = '?')) then
```

```
    length = i - start
```

```
    start = i+1
```

```
    sum = sum + length
```

```
    if length > max then
```

```
      max = length
```

```
    end if;
```

```
    if length < min then
```

```
      min = length
```

```
    end if;
```

```
    MEM_D[count] = length
```

```
    count ++;
```

```
  end if;
```

```
  i++
```

```
end while
```

```
avr = sum/2048
```

```
done = 1
```

```
wait for s=0
```

```
// when s=0, an external circuit can read data from memory MEM_D, one number at a time,
```

```
// using ports mem_addr and mem_dout
```

```
go to begin
```

Please clearly mark widths of all buses in your circuit.

Assume the following interface to your circuit:

Port	Width	Meaning
clk	1	System clock.
reset	1	System reset – clears all internal registers and counters. Active high.
din	8	Input data bus.
s	1	Operating mode: 0 = waiting for data/reading results, 1 = processing.
rd	1	Read enable. 0 = high impedance on the output bus dout, 1 = valid output dout
dout	10	One of the three results calculated by the circuit.
sel_out	2	Selection between the three calculated results: 0 = avr, 1 = max, 2 = min.
mem_addr	11	Address in memory location MEM_D.
mem_dout	10	High impedance (if s=1) or value of memory location MEM_D[mem_addr] (if s=0).
done	1	Asserted when all results are ready, zero otherwise

Problem 2 (7.5 points)

1. Draw an ASM chart corresponding to the pseudocode from Problem 1.
2. Express all operations in your ASM chart in terms of active values of control signals generated as outputs of the Control unit and used as inputs in the Datapath.

Problem 3 (7 points)

Determine the contents of

1. Internal registers s0-s6
2. Flags C, Z
3. Flags I, preserved C, and preserved Z
4. PC
5. Stack
6. External RAM
7. Data RAM

at the time of the execution of the instruction

RETI DISABLE

before this instruction takes effect assuming that

- The PicoBlaze system contains external RAM visible by PicoBlaze in the I/O address range 0x00..0xFF
- The PicoBlaze runs at the clock frequency of 100 MHz
- The generic interrupt_vector is set to X"FFF", and scratch_pad_memory_size to 256
- at the time = 0 a short pulse is generated at the input reset
- at the time = 20 microseconds, a short pulse is generated at the input interrupt
- the contents of the instruction memory is given by the following program:

```

BIT0    EQU    0x01
BIT6    EQU    0x40

        ORG 0x000
        JUMP START

        ORG 0x400
START:  LOAD s0, 0x00
        LOAD s1, 0x01
        LOAD s2, 0x02

INIT:   OUT    s1, (s0)
        STORE s2, (s0)
        ADD   s2, 0x01
        ADD   s1, 0x01
        ADD   s0, 0x01
        JUMP  NC, INIT
        EINT

        FETCH s3, 0xFF
        IN    s4, 0xFD
        ADD   s3, s4

        CALL SUB1
        JUMP LOOP

SUB1:   CALL SUB2
        JUMP LOOP

SUB2:   CALL LOOP
        JUMP START

LOOP:   JUMP LOOP

        ORG 0x800
ISR:    IN    s5, 0xFE
        LOAD  s6, 0xAE
        XOR   s6, BIT0
        OR    s6, BIT6
        TEST  s5, s6
        SRX   s6
        RETI  DISABLE

        ORG 0xFFF
        JUMP ISR

```

Problem 4 Bonus (3 bonus points)

Draw a detailed block diagram of the digital system including

1. the PicoBlaze 6 core, KCPSM6
2. the instruction ROM required for the basic operation of the PicoBlaze core
3. 32 x 8 external data RAM visible under addresses 0x40-0x5F
4. 32 x 8 external data ROM visible under addresses 0x60-0x7F
5. two input registers with the virtual addresses 0x80 and 0x81
6. two output registers with the virtual addresses 0x80 and 0x91

Assume that

- input register with the address 0x80 is the same as the output register with the address 0x80
- the input and output registers, data RAM, and data ROM specified above are the only i/o devices that the PicoBlaze core is communicating with
- your system needs to be able to allow the PicoBlaze core to write to all aforementioned output registers and data RAM, and read from all the aforementioned input registers, data RAM, and data ROM, using instructions OUT and IN, respectively
- you need to provide all details of the address decoder, and build it out of basic logic components you are familiar with
- all registers and flip-flops have a reset input connected to the external port RESET.

Please clearly mark on your schematic:

- sizes of all memories and registers
- sizes and directions of all buses.