Midterm Exam ECE 448

Spring 2014

Monday, March 3

(15 points)

Instructions:

Zip all your deliverables into an archive <last_name>.zip and submit it through Blackboard no later than Monday, March 3, 10:15 PM EDT.

Lab Midterm Exam

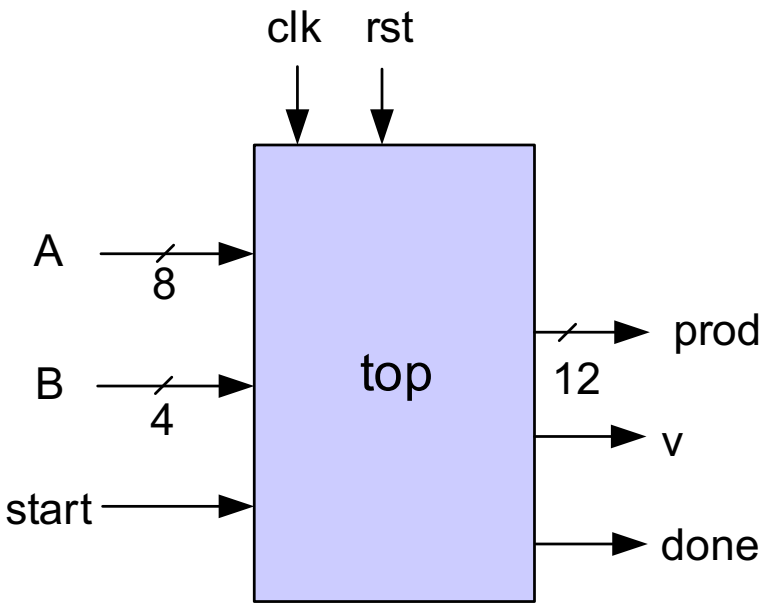
The circuit described below performs the multiplication operation in the binary format, and then expresses the result in the BCD format. The design accepts an 8-bit unsigned multiplicand and a 4-bit unsigned multiplier. It produces a 12-bit result in BCD format. Signal "start" is used to initiate the operation.

The circuit is specified below using its:

- Interface
- Table of input/output ports
- Block diagram
- Test vectors
- Timing waveforms from functional simulation

Top-level view of Multiplier:

Assume the following top-level view to your circuit.



Assume the following division of your circuit into the Datapath and Controller.

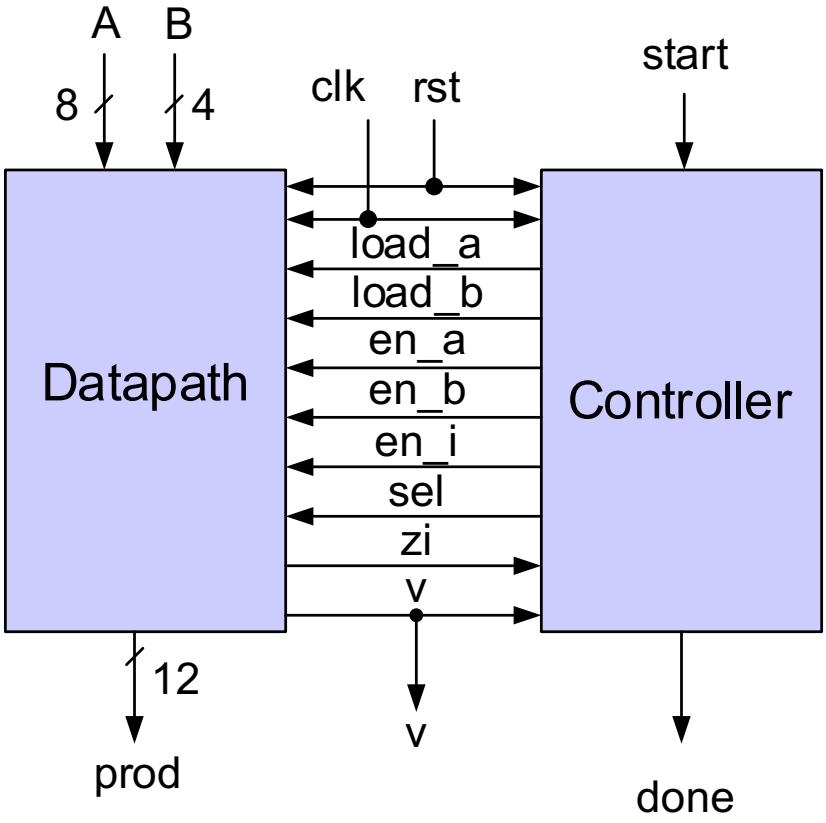
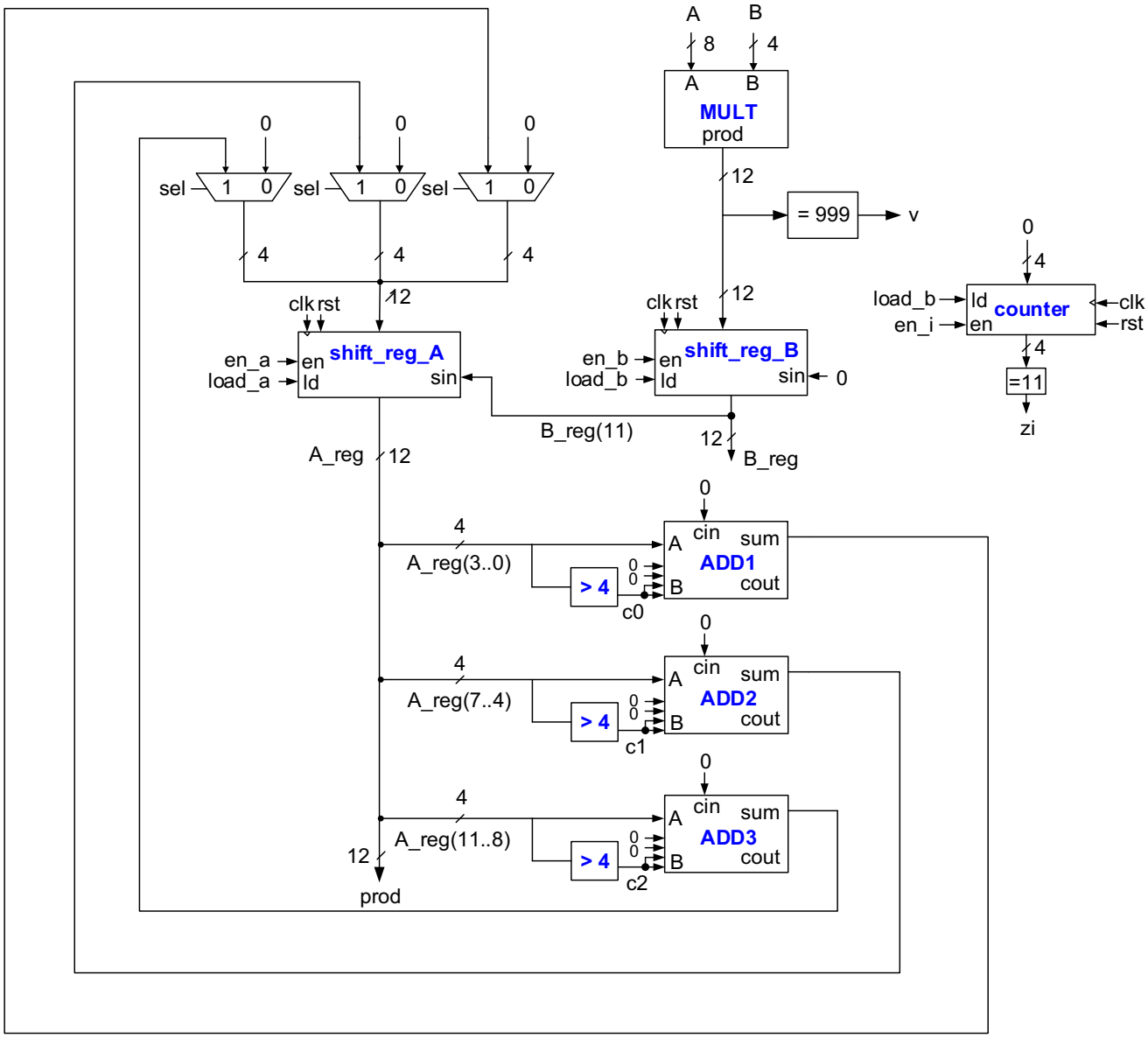


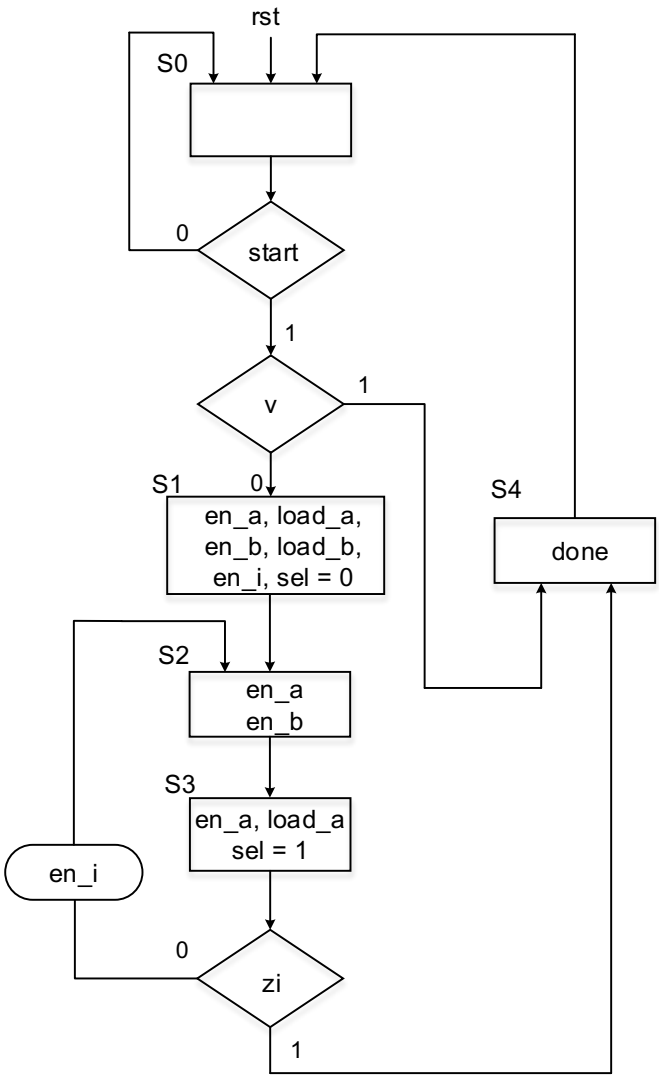
Table of input/output ports:

Port	Mode	width	Function
clk	IN	1	System clock
rst	IN	1	Asynchronous system reset
A	IN	8	Multiplicand
B	IN	4	Multiplier
start	IN	1	A signal to initiate multiplication operation
prod	OUT	12	Result of the multiplication in BCD format
done	OUT	1	A signal to show the end of operation

Block diagram:



ASM Chart:



Test vectors:

Inputs:

A = x"4E" = 78 (in decimal)
B = x"9" = 9 (in decimal)

Output:

prod = x"2BE" = 702 (in decimal)
v=0

Inputs:

A = x"AB" = 171 (in decimal)
B = x"9" = 9 (in decimal)

Output:

prod = undefined (out of range)
v=1

Design Requirements:

The combinational portion of the circuit should be described using the dataflow VHDL code, and the sequential portion of the circuit should be described using the synthesizable behavioral code. Your code should infer a circuit that requires a minimum amount of FPGA resources. The target clock frequency should be **100 MHz**.

Tasks:
Perform the following tasks:

1. Write a synthesizable VHDL code representing the multiplication circuit
2. Write a testbench verifying the operation of your circuit.
3. Perform functional simulation of your circuit and use it to debug your VHDL code. Take a print out of the waveform showing the entire operation using default PDF conversion tool installed in the lab (Use multiple page option in order to display necessary information on multiple pages, if required).
4. Synthesize your circuit.
5. Implement your circuit using
    a. FPGA family: Spartan 6
    b. Device: x c 6 s l x 1 6 - 3 c s g 3 2 4
    c. Speed Grade: -3
6. Run the static timing analysis of your circuit.
7. Based on the circuit block diagram and the report from the static timing analysis, determine the most critical path in your circuit and the circuit maximum clock frequency.
8. Based on the implementation reports, determine the number of CLB slices, LUTs, flip-flops, and pins used by the circuit.
9. Perform the timing simulation of your circuit at the maximum clock frequency returned by the static timing analysis. Take a printout of the waveform showing the entire operation using default PDF conversion tool installed in the lab (Use multiple page option in order to display necessary information on multiple pages, if required).

Deliverables:

1. VHDL code of your entire circuit fulfilling the requirements specified in the *Design Requirements* section above.
2. VHDL code of your testbench.
3. Timing waveforms from the functional and timing simulations demonstrating the correct operation of your circuit.
4. Description of the critical path in your circuit
5. FPGA resource utilization (as defined in Task 8 above).
6. Minimum clock period and maximum clock frequency of your circuit.