ECE 448
Midterm Exam
Monday, March 2, 2015

Problem 1 (25%)

Given the controller, described using the ASM chart shown in Fig. 1:

A. supplement timing waveforms provided in the answer sheet with the values of the **state S**, and the values of the **outputs x**, **y**, and **z**
B. write the VHDL **dataflow** code **for the output function (only)**, calculating **x**, **y**, and **z**.

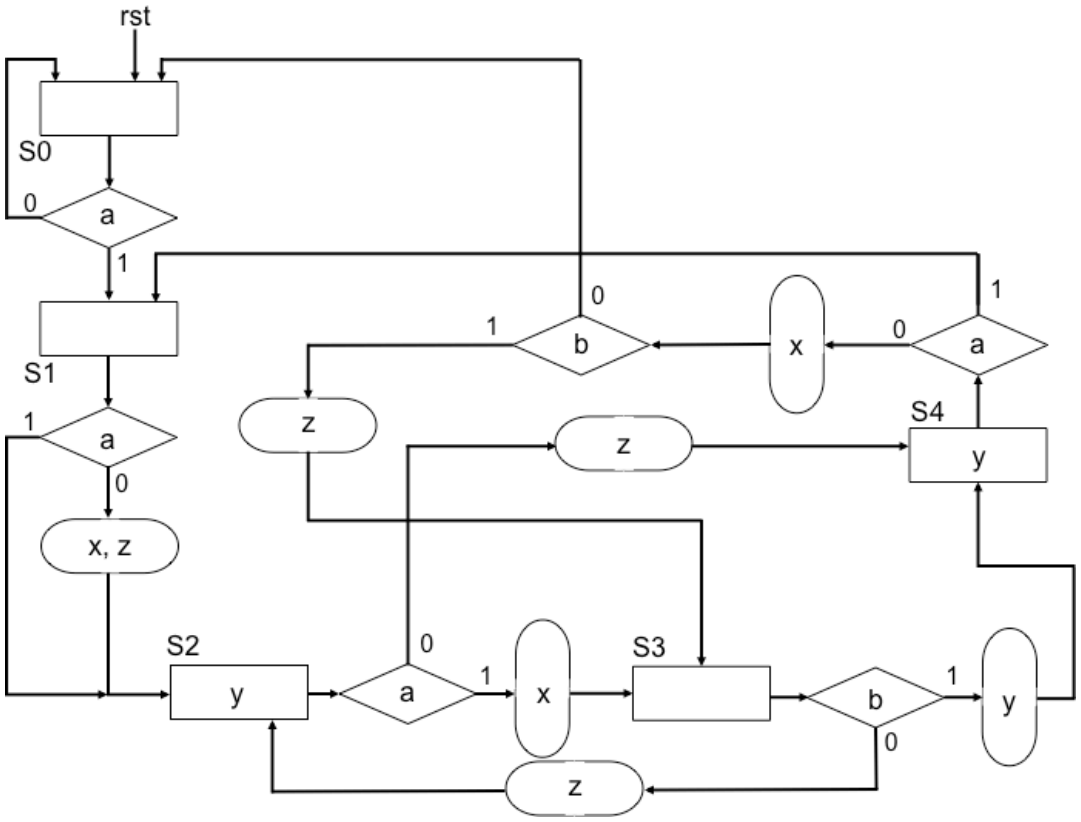

Fig. 1: ASM chart of the controller.

Problem 2 (25%)

Draw block diagrams of

A. 3-to-8 decoder (with enable) built of 2-to-4 decoders (with enable) and a minimum number of logic gates
B. 5-bit priority encoder built of 2-to-1 multiplexers and a minimum number of logic gates (assume that the least significant bit of the input **w** has the highest priority, and the **z** output is equal to 1 when at least one input bit is equal to 1).
C. 128x1 RAM built of two 64x1 RAMs and a minimum number of logic gates.
D. 4-bit shift register with the serial input sin, enable en, clock clk, and the serial output sout.

For each of the above circuits determine

- the minimum number of Spartan 6 LUTs necessary to implement a given circuit,
- a mode in which each of these LUTs must be configured (ROM, RAM, or SR).

Problem 3 (25%)

Write the full VHDL code of the Variable Arithmetic Shifter Right, shown in Fig. 2, performing the operation Z = X >> Y, for the 16-bit signed number X, and the 8-bit unsigned number Y. **Assume that you are not allowed to use any predefined library functions for a fixed shift or a variable shift. Do your best to minimize the length of your code by using the for-generate statement.**

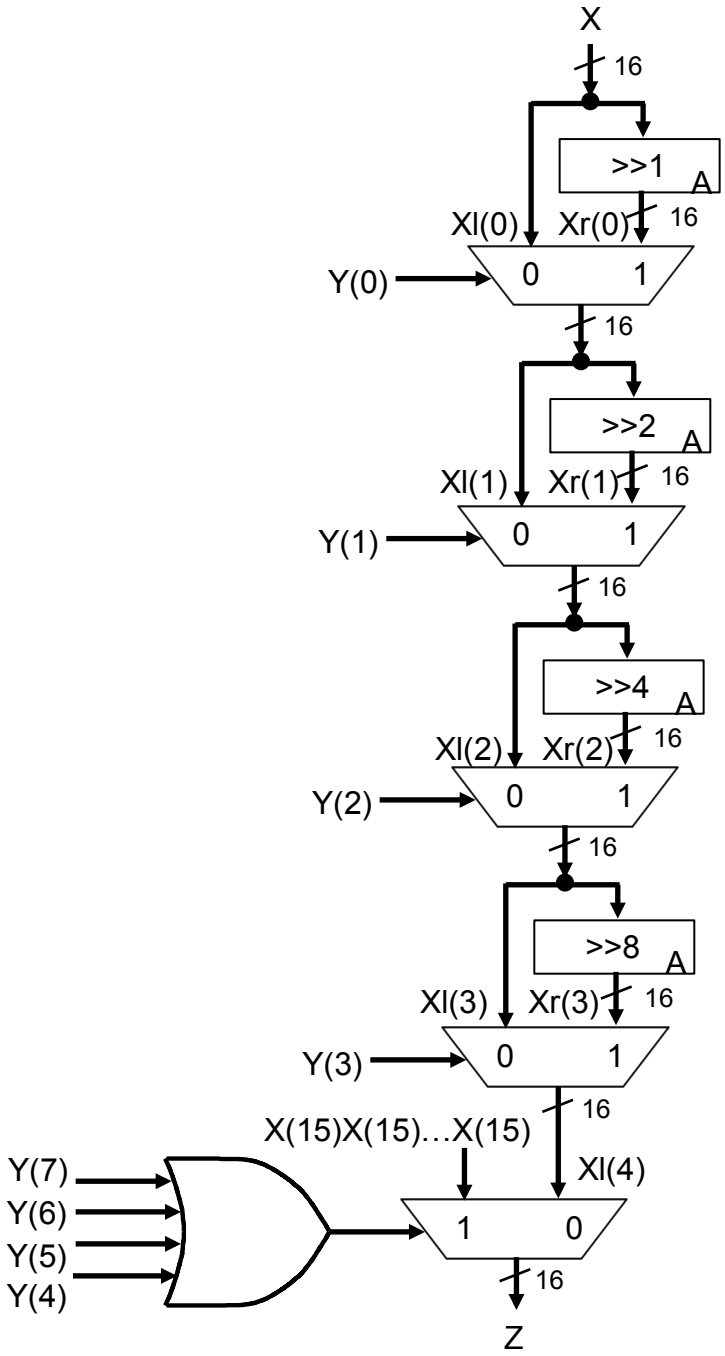

Fig. 2: Block diagram of the Variable Arithmetic Shifter Right, Z=X>>Y.

Problem 4 (25%)

Write a complete simple testbench capable of generating inputs **rst**, **clk**, **a**, and **b** to the Controller described by the ASM chart shown in Fig. 1, changing according to the timing waveforms shown in Fig. 3.

Assume that the signals:

- **clk** and **a** are periodical
- **rst** and **b** are non-periodical.

Please note that your testbench should include the instantiation of the Controller, defined in Problem 1.

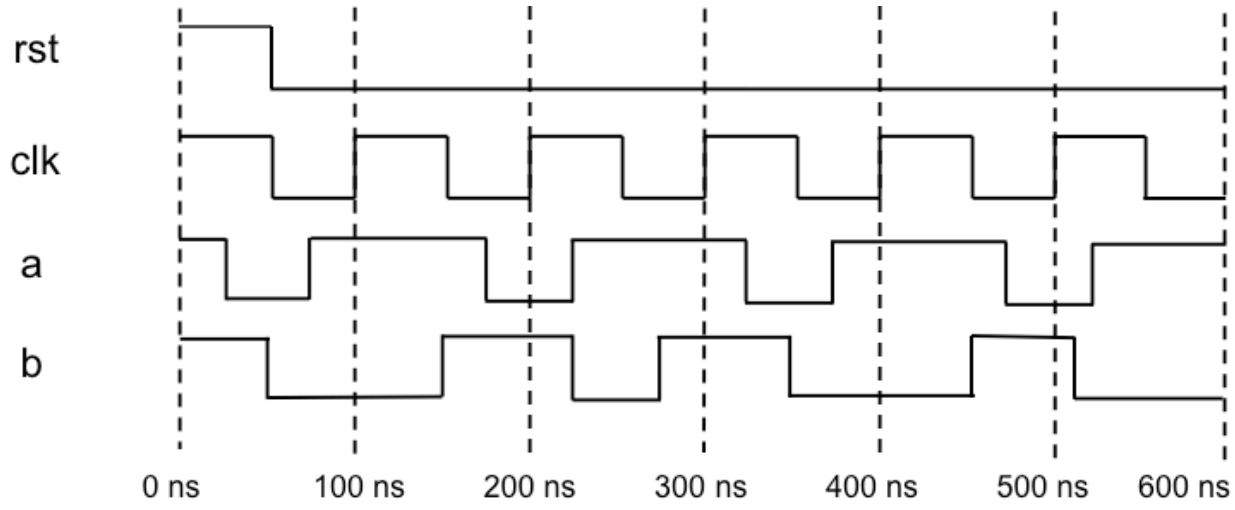

Fig. 3: Timing Waveforms of the Controller Inputs.