ECE 448
Final Exam – Part 1
Spring 2015

First name:
Last name:

1. How many data words of the size of 32 bits can be held in a single Block RAM in Spartan 6 FPGA?

How many parity bits can accompany each data word?

2. What is a primary application of two register banks in PicoBlaze-6?

How can programmer switch between using Bank A and Bank B?

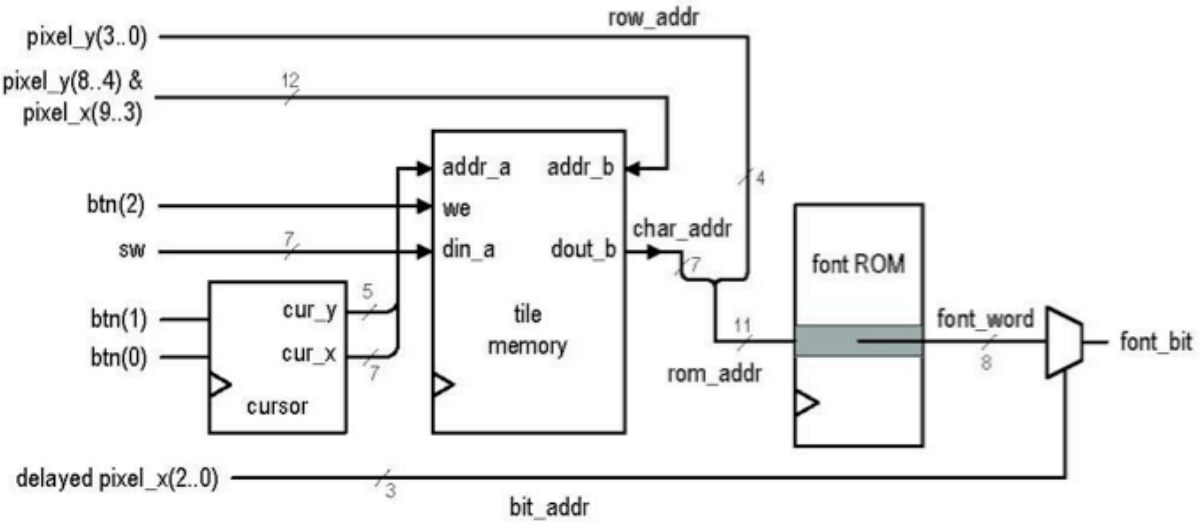
3. What is a direction, width, and function of the following ports of PicoBlaze-6?

A. **port_id**

B. bram_enable

C. sleep

4. Based on the given below block diagram of the Text Generation Circuit with Tile Memory, provide the following information about the <u>tile memory</u>:



A. **Type of memory (RAM or ROM, single-port or dual-port): …….**
   …….
B. **Total number of words (locations in memory): …….**
C. **Size of each word (location in memory): …….**
D. **Total size of memory in kbits: …….**
E. **Number of words used to hold ASCII codes of tiles: …….**
F. **Utilization of memory in % (E/B*100%) …….**
G. **Address of the location holding ASCII code of the tile with coordinates (0, 1), i.e., the first tile of the second row: …….**