Final Exam – Part 2
Spring 2015

Problem 1 (7 points)

Draw a block diagram of the datapath unit of a circuit capable of executing the pseudocode given below.

In this code, MEM_A and MEM_B represent two single-port memories of the size of 256 x 32. These memories are initialized using a burst mode with the burst size equal to 256. The beginnings of the bursts are indicated with active values of inputs burst_A and burst_B, respectively. The start of calculations is indicated with the active value of the input s. The results are written to an output FIFO, as soon as this FIFO is not full.

```
begin:

done = 0

wait for burst_A=1
for i = 0 to 255 do
  MEM_A[i] = dina
end for

wait for burst_B=1
for i = 0 to 255 do
  MEM_B[i] = dinb;
end for

wait for s=1

for i = 0 to 255 do
    if (MEM_A[i] ≥ MEM_B[i]) then
        X =  MEM_A[i]
        Y =  MEM_B[i]
    else
        X =  MEM_B[i]
        Y =  MEM_A[i]
        MEM_A[i] = X
        MEM_B[i] = Y
    end if

   SUM_MAX = SUM_MAX + X
   SUM_MIN   = SUM_MIN + Y
end for

AVR_MAX = SUM_MAX / 256
AVR_MIN =  SUM_MIN  /  256
GT_AVR_MAX = 0
GT_AVR_MIN = 0
```

```
for i = 0 to 255 do
     if  MEM_A[i] > AVR_MAX then
          GT_AVR_MAX++
     end if
     if  MEM_B[i] > AVR_MIN then
          GT_AVR_MIN++
     end if
     MEM_A[i] = MEM_A[i] – AVR_MAX
     MEM_B[i] = MEM_B[i] – AVR_MIN
 end for

for i = 0 to 255 do
   wait for fifo_full = 0
   write MEM_A[i] to fifo
end for

for i = 0 to 255 do
   wait for fifo_full = 0
   write MEM_B[i] to fifo
end for

done = 1
wait for s=0
go to begin
```

Please clearly mark the widths of all buses in your circuit.

Assume the following interface to your circuit:

Port	Dir	Width	Meaning
clk	In	1	System clock.
reset	In	1	System reset – clears all internal registers and counters. Active high.
s	In	1	Operating mode: 0 = initialization/reading results, 1 = processing.
dina	In	32	Input data bus for MEM_A
dinb	In	32	Input data bus for MEM_B
burst_A	In	1	Start of the burst at input dina
burst_B	In	1	Start of the burst at input dinb
dout_fifo	Out	32	Output data bus connected to an external FIFO
wr_fifo	Out	1	Writing data to an external fifo
fifo_full	In	1	External FIFO full
dout	Out	8	Output data bus
rd	In	1	External read enable for the output dout. 0 = high impedance on the output bus dout, 1 = valid output dout
sel	In	1	Valid output = GT_AVR_MAX for sel=0, and GT_AVR_MIN for sel=1
done	Out	1	Asserted when all results are ready, zero otherwise

Problem 2 (7 points)

1. Draw an ASM chart corresponding to the pseudocode from Problem 1.
2. Express all operations in your ASM chart in terms of active values of control signals generated as outputs of the Control unit and used as inputs in the Datapath.

Problem 3 (7 points)

Determine the contents of

1. Internal registers s0-s6
2. Flags C, Z
3. Flags I, preserved C, and preserved Z
4. PC
5. Stack
6. External RAM
7. Data RAM

at the time of the execution of the instruction

RETI DISABLE

before this instruction takes effect assuming that

- The PicoBlaze system contains external RAM visible by PicoBlaze in the I/O address range 0x00..0xFF
- The PicoBlaze runs at the clock frequency of 100 MHz
- The generic interrupt_vector is set to X"FFF", and scratch_pad_memory_size to 256
- at the time = 0 a short pulse is generated at the input reset
- at the time = 20 microseconds, a short pulse is generated at the input interrupt
- the contents of the instruction memory is given by the following program:

```
BIT0        EQU   0x01
BIT7        EQU   0x80

            ORG 0x000
            JUMP START

ISR:
            IN        s5, 0x80
            LOAD      s6, 0xA0
            XOR       s5, BIT0
            OR        s6, BIT7
            TEST      s5, s6
            RL        s6
            RETI      DISABLE

            ORG 0x400
START:
            LOAD s0, 0xAC
            LOAD s1, 0x80
            LOAD s2, 0x08
```

```
INIT:
        OUT     s0, (s1)
        STORE   s2, (s1)
        ADD     s0,  0x04
        ADD     s1, 0x20
        SUB     s2, 0x02
        JUMP    NZ, INIT
        EINT

        FETCH  s3, 0xE0
        IN      s4, 0xC0
        SUB     s4, s3

        CALL SUB1
        JUMP LOOP

        ORG 0x600
SUB1:
        CALL SUB2
        JUMP LOOP

        ORG 0x700
SUB2:
        CALL LOOP
        JUMP START

        ORG 0x800
LOOP:
        JUMP  LOOP

        ORG 0xFFF
        JUMP ISR
```

Problem 4 Bonus (3 bonus points)

Draw a detailed block diagram of the digital system including

1. the PicoBlaze 6 core, KCPSM6
2. the instruction ROM required for the basic operation of the PicoBlaze core
3. 32 x 8 external data RAM visible under addresses 0x80-0x9F
4. 64 x 8 external data ROM visible under addresses 0xC0-0xFF
5. two input registers with the virtual addresses 0x04 and 0x08
6. two output registers with the virtual addresses 0x08 and 0x0C
7. a D flip-flop with the output Q connected to the interrupt input of the PicoBlaze core, input SET connected to the external port INT, and input CLR connected to an appropriate output of the PicoBlaze core.

Assume that

- input register with the address 0x08 is the same as the output register with the address 0x08

- the input and output registers, data RAM, and data ROM specified above are the only i/o devices that the PicoBlaze core is communicating with
- your system needs to be able to allow the PicoBlaze core to write to all aforementioned output registers and data RAM, and read from all the aforementioned input registers, data RAM, and data ROM, using instructions OUTPUT and INPUT, respectively
- you need to provide all details of the address decoder, and build it out of basic logic components you are familiar with
- all registers and flip-flops have a reset input connected to the external port RESET.

Please clearly mark on your schematic:

- sizes of all memories and registers
- sizes and directions of all buses.