ECE 448
Midterm Exam
Monday, February 29, 2016

Problem 1 (25%)

Given the controller, described using the ASM chart shown in Fig. 1:

A. supplement timing waveforms provided in the answer sheet with the values of the **state S**, and the values of the **outputs p**, **r**, and **y**
B. write the VHDL **behavioral** code **for the next state function (only)**, calculating value of the next state S.

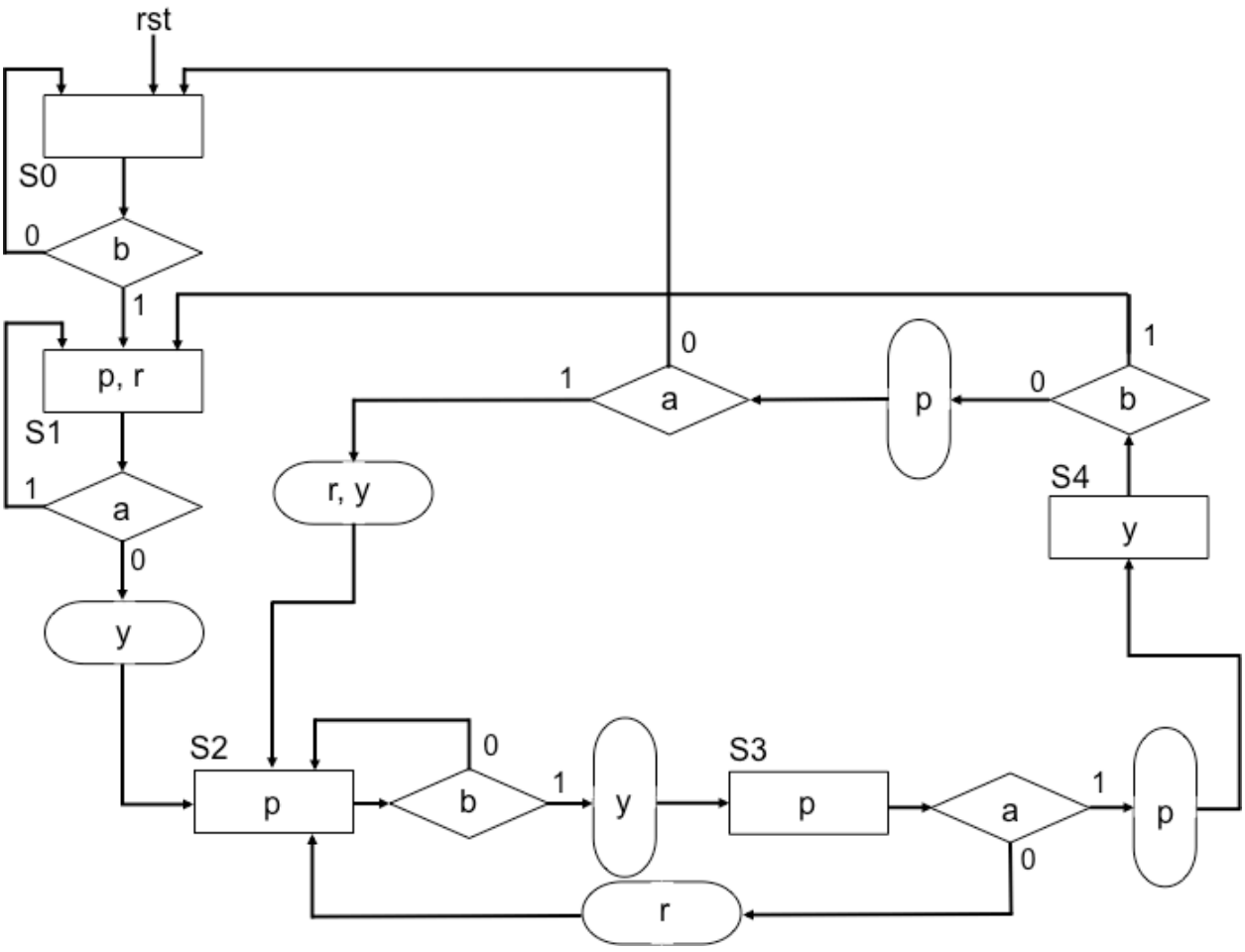

Fig. 1: ASM chart of the controller.

Problem 2 (25%)

Draw block diagrams of

A. a circuit that calculates the majority function of 4 variables, x3, x2, x1, x0, built using a ROM. On a separate diagram, show the full contents of the ROM.
B. a circuit that calculates a maximum of two 4-bit signed inputs A and B, built of comparators and multiplexers.
C. 64x4 RAM built of four 64x1 RAMs.
D. 4-bit shift register with the parallel input D, the serial input sin, load ld, enable en, clock clk, and the serial output sout. Assume that an active value of ld and the rising edge of clk

are sufficient for the load to take place, sin is connected to the least significant stage of the shift register, and sout is connected to the most significant stage of the shift register.

For each of the above circuits determine

- the minimum number of Spartan 6 LUTs necessary to implement a given circuit,
- a mode in which each of these LUTs must be configured (ROM, RAM, or SR).

Problem 3 (25%)

Draw a block diagram of the digital circuit with the following interface and functionality:

Interface:
DIN – 8-bit data input
DOUT – 8-bit data output
ADDR – 2-bit address of the location (register) where input data is stored or output data is read from
RW– control signal, 0=read, 1=write
CLK – clock
Functionality:
If RW = 1, then at the next rising edge of the clock, data from the input DIN is stored in the internal location given by the address ADDR, and the output DOUT is set to the high impedance state.
If RW = 0, data from the location given by the address ADDR is transferred to the output DOUT, the contents of the internal memory (registers) does not change.

Assume that the internal memory is implemented using registers.
Use only medium scale components, such as registers, multiplexers, encoders, decoders, buffers, etc.

Write VHDL code of the architecture of this circuit using dataflow VHDL only.

Problem 4 (25%)

Write a **complete simple testbench** capable of verifying the operation of MISR (Multiple Input Signature Register) shown in Fig. 2.

The testbench should instantiate MISR, using the VHDL-93 convention, with the value of the generic C equal to X"B8". Assume that the name of the MISR entity is MISR, and the name of its architecture is behavioral.

The test should consist of

1. resetting MISR
2. applying 128 inputs D, varying between X"00" and X"FE" with the step of 2 (i.e., values X"00", X"02", X"04", …, X"FE"), one per clock cycle, with the input en active
3. deactivating en for 10 clock cycles
4. applying 128 inputs D, varying between X"01" and X"FF" with the step of 2 (i.e., values X"01", X"03", X"05", …, X"FF"), one per clock cycle, with the input en active.
5. deactivating en.

Assume that all external inputs should be changed on the falling edges of the clock.

After step 5, all inputs (other than clk) should remain stable (i.e., keep their last value) till the end of simulation.

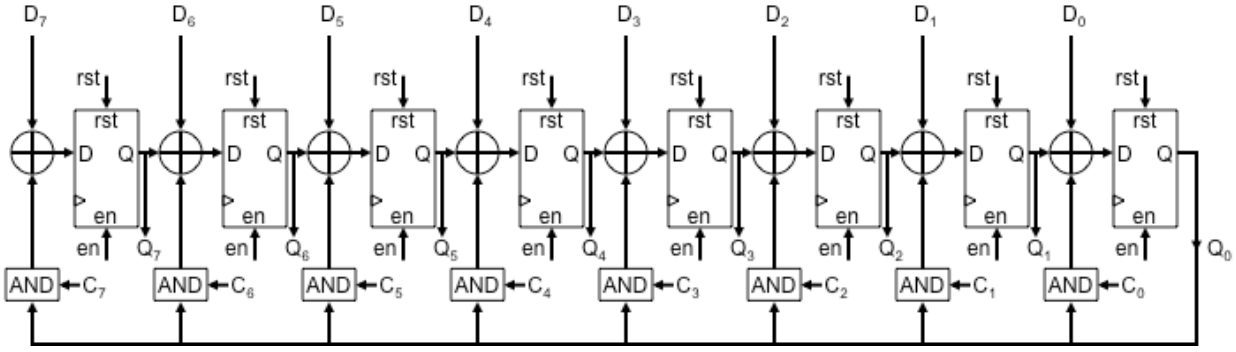

Fig. 2: Block Diagram of Multiple Input Shift Register.