Midterm Exam ECE 448
Spring 2016
Monday, March 14
15 points

Instructions:
Zip all your deliverables into an archive <last_name>.zip and submit it through Blackboard no later than Monday, March 14, 7:20 PM EDT.

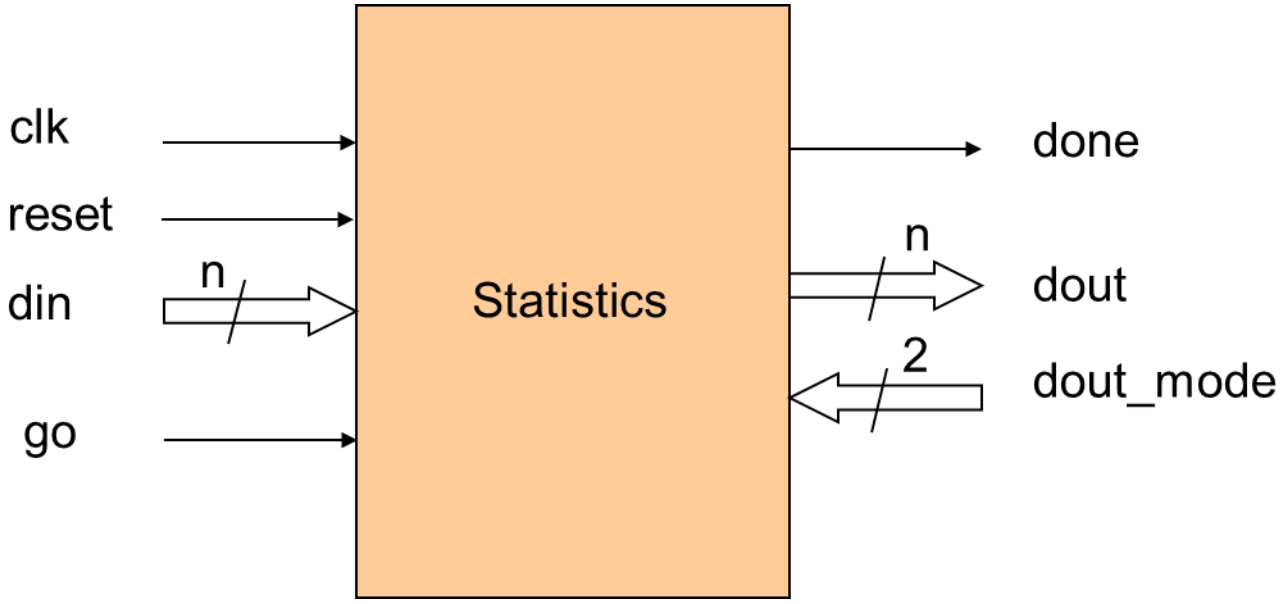
The circuit described below is STATISTICS circuit which is capable of computing the first three largest numbers in the set of $k=2^m$ n-bit unsigned numbers provided at its input. In parallel, the circuit should also compute an average of all k inputs.

The circuit is specified below using its:

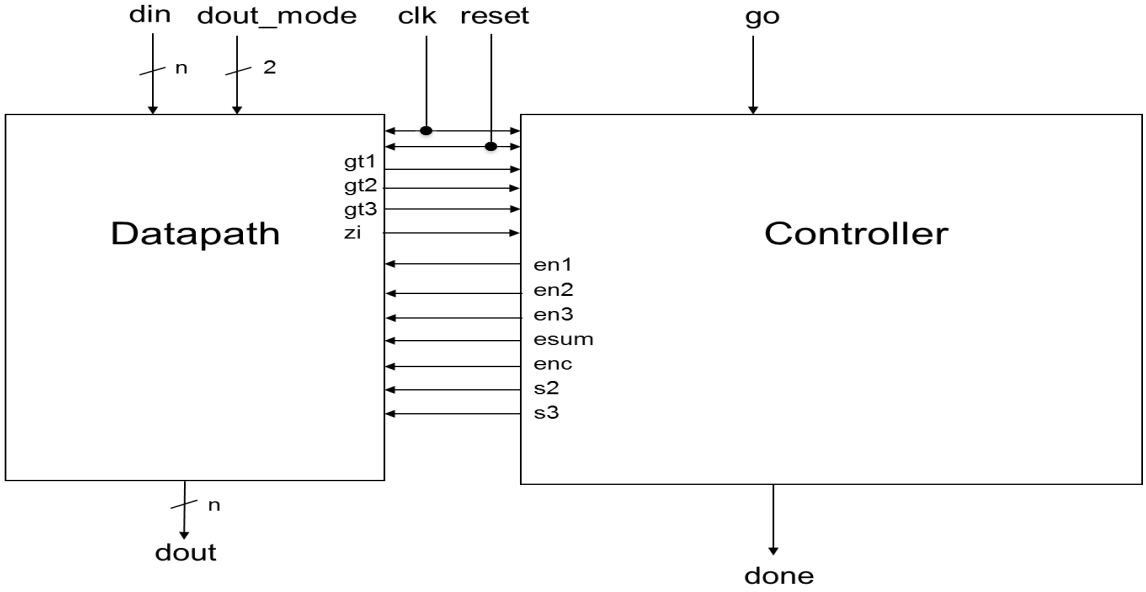
- Top Level
- Interface
- Pseudocode
- Table of input/output ports
- Block diagram of Datapath and ASM.

Top Level- Statistics Circuit

Assume the following top-level view to your circuit.



Interface of Statistics Circuit:



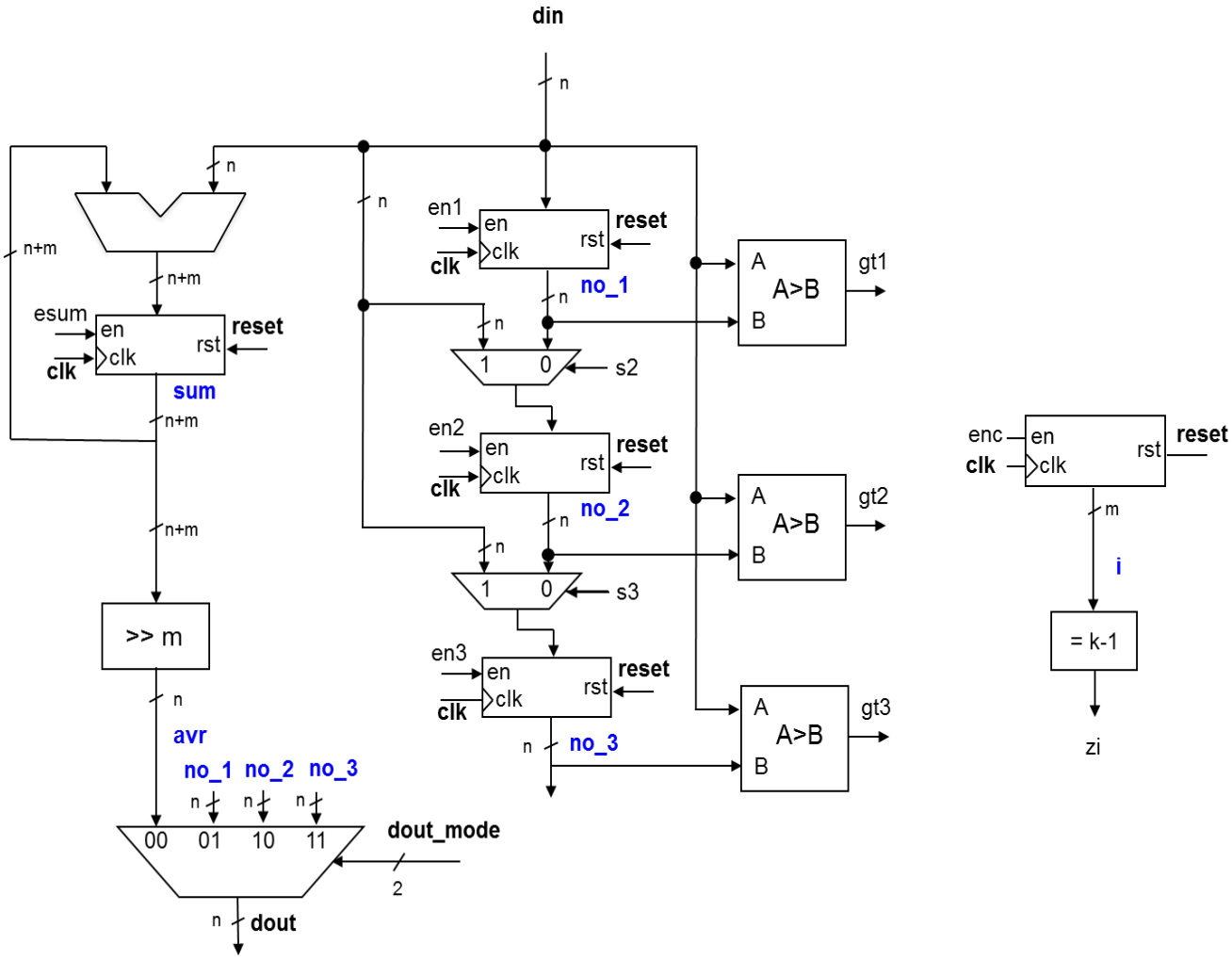
Pseudocode

```
no_1 = no_2 = no_3 = sum = 0
for i=0 to k-1 do
        sum = sum + din
        if  din > no_1 then
                no_3 = no_2
                no_2 = no_1
                no_1 = din
        elseif (din > no_2) then
                no_3 = no_2
                no_2 = din
        elseif (din > no_3) then
                no_3 = din
        end if
end for
avr = sum / k
```

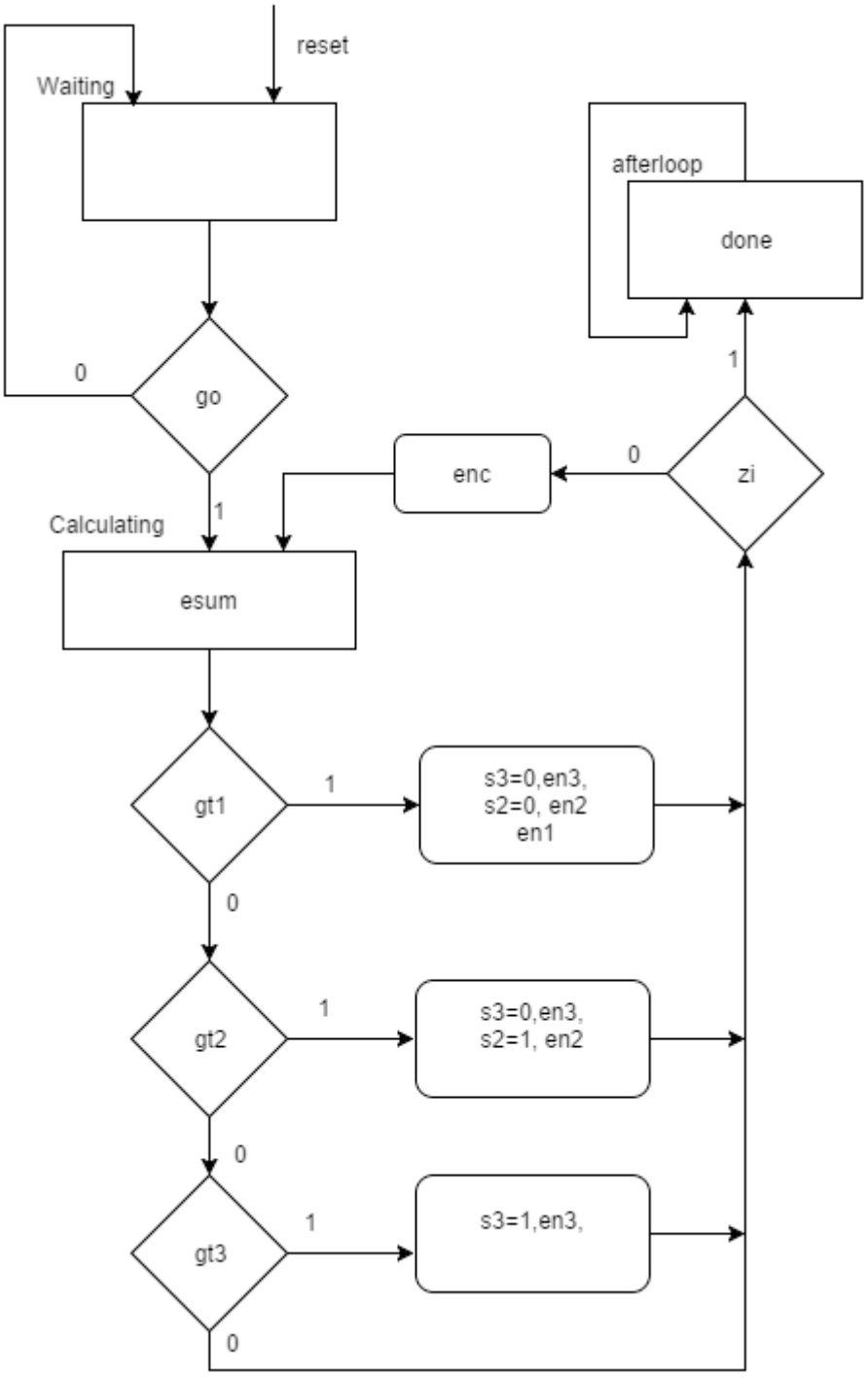
Table of input/output ports

Port	Width	Meaning
clk	1	System clock.
reset	1	System reset. Active high.
din	n	Input Data.
go	1	Control signal indicating that the first input is ready. Active for one clock cycle.
done	1	Signal set to high after the output is ready.
dout	n	Output dependent on the dout_mode input.
dout_mode	2	Control signal determining value available at the output. 00: avr, 01: no_1, 10: no_2, 11: no_3.

Block Diagram of Datapath



ASM


reset
Waiting
afterloop
done
0
go
1
0
enc
zi
Calculating
1
esum
gt1
1
s3=0,en3,
s2=0, en2
en1
0
gt2
1
s3=0,en3,
s2=1, en2
0
gt3
1
s3=1,en3,
0

Tasks:
Perform the following tasks:

1. Write a synthesizable VHDL code representing the Statistics circuit
2. Write a testbench verifying the operation of your circuit.
3. Perform functional simulation of your circuit and use it to debug your VHDL code. Take a print out of the waveform showing the entire operation using default PDF conversion tool installed in the lab (Use multiple page option in order to display necessary information on multiple pages, if required).
4. Synthesize your circuit.
5. Implement your circuit using
    a. FPGA family: Spartan 6
    b. Device: x c 6 s l x 1 6 -3csg324
    c. Speed Grade: -3
6. Run the static timing analysis of your circuit.
7. Based on the circuit block diagram and the report from the static timing analysis, determine the most critical path in your circuit and the circuit maximum clock frequency.
8. Based on the implementation reports, determine the number of CLB slices, LUTs, flip-flops, and pins used by the circuit.
9. Perform the timing simulation of your circuit at the maximum clock frequency returned by the static timing analysis. Take a printout of the waveform showing the entire operation using default PDF conversion tool installed in the lab (Use multiple page option in order to display necessary information on multiple pages, if required).

Deliverables:
1. VHDL code of your entire circuit fulfilling the requirements specified in the *Design Requirements* section above.
2. VHDL code of your testbench.
3. Timing waveforms from the functional and timing simulations demonstrating the correct operation of your circuit.
4. Description of the critical path in your circuit
5. FPGA resource utilization (as defined in Task 8 above).
6. Minimum clock period and maximum clock frequency of your circuit.