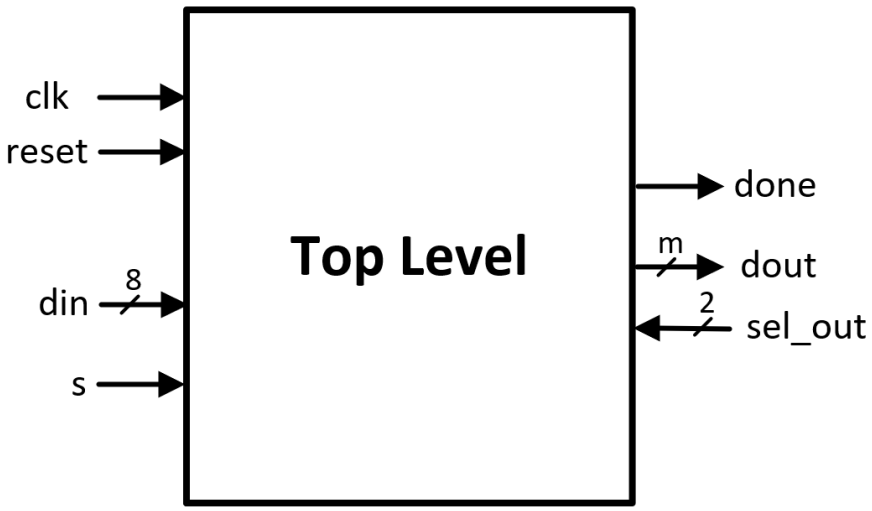
Midterm Exam ECE 448
Spring 2019
Tuesday, March 5
15 points

Instructions:
Zip all your deliverables into an archive <last_name>.zip and submit it through Blackboard no later than Tuesday, March 5, 11:40 AM EST.

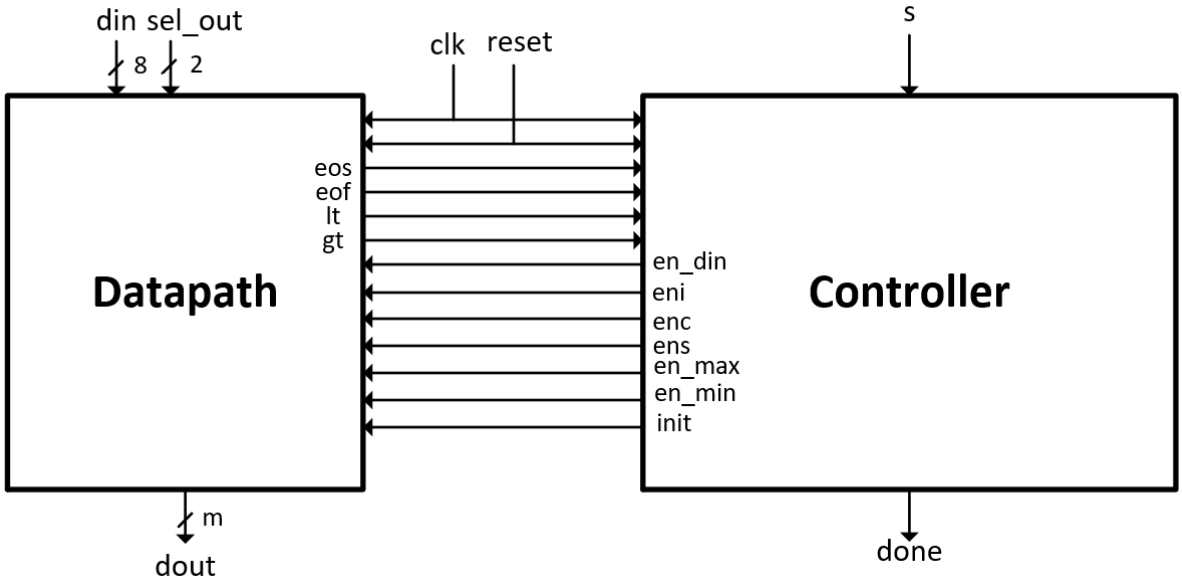
The EXAM circuit takes as an input a stream of 8-bit ASCII characters representing a document written in English. It calculates the lengths of 2^n first sentences (i.e., strings ending with '.', '?', or '!'). In parallel, it calculates the minimum, maximum, and average length of a sentence in the input text. The document is assumed to contain at least 2^n sentences. All sentences are assumed to be shorter than 2^m characters.
The circuit is specified below using its:

- Top-level circuit interface
- Interface with the division into the Datapath and Controller
- Pseudocode
- Table of input/output ports
- Block diagram of the Datapath
- ASM chart of the Controller.

Top-level circuit interface



Interface with the division into the Datapath and Controller



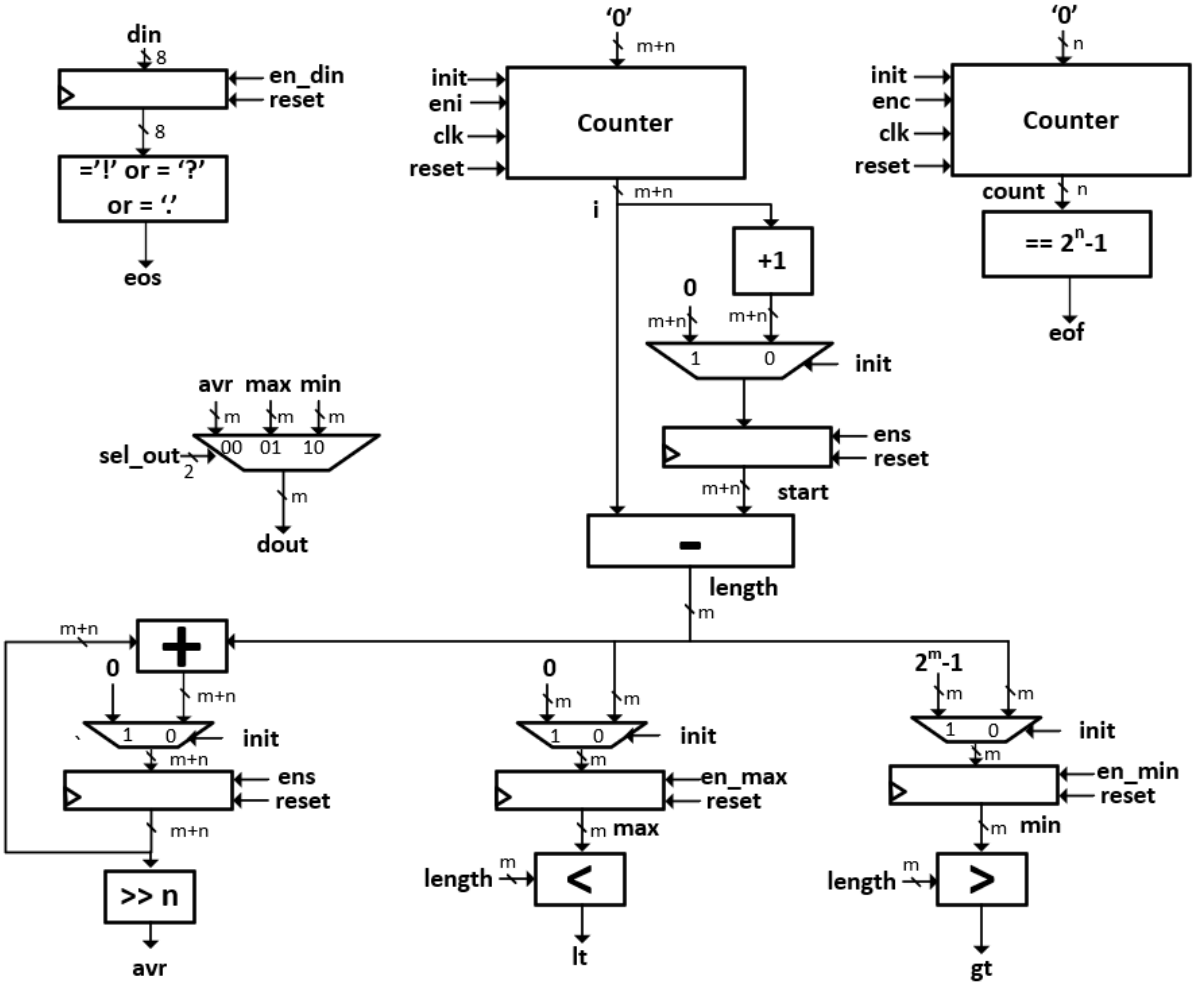
Pseudocode

```
begin:

wait for s=1
done = 0
i=0; count = 0
start = 0
sum=0; max=0; min=2^m-1

while (count < 2^n) do
      next = din
      if ((next = '.') or (next = '!') or (next = '?')) then
            length = i - start
            start = i+1
            sum = sum + length
            if length > max then
                  max = length
            end if;
            if length < min then
                  min = length
            end if;
            count ++;
      end if;
      i++
end while

avr = sum/2^n

done = 1
wait for s=0
// when s=0, an external circuit can read the maximum, minimum or
// average sentence length.
go to begin
```

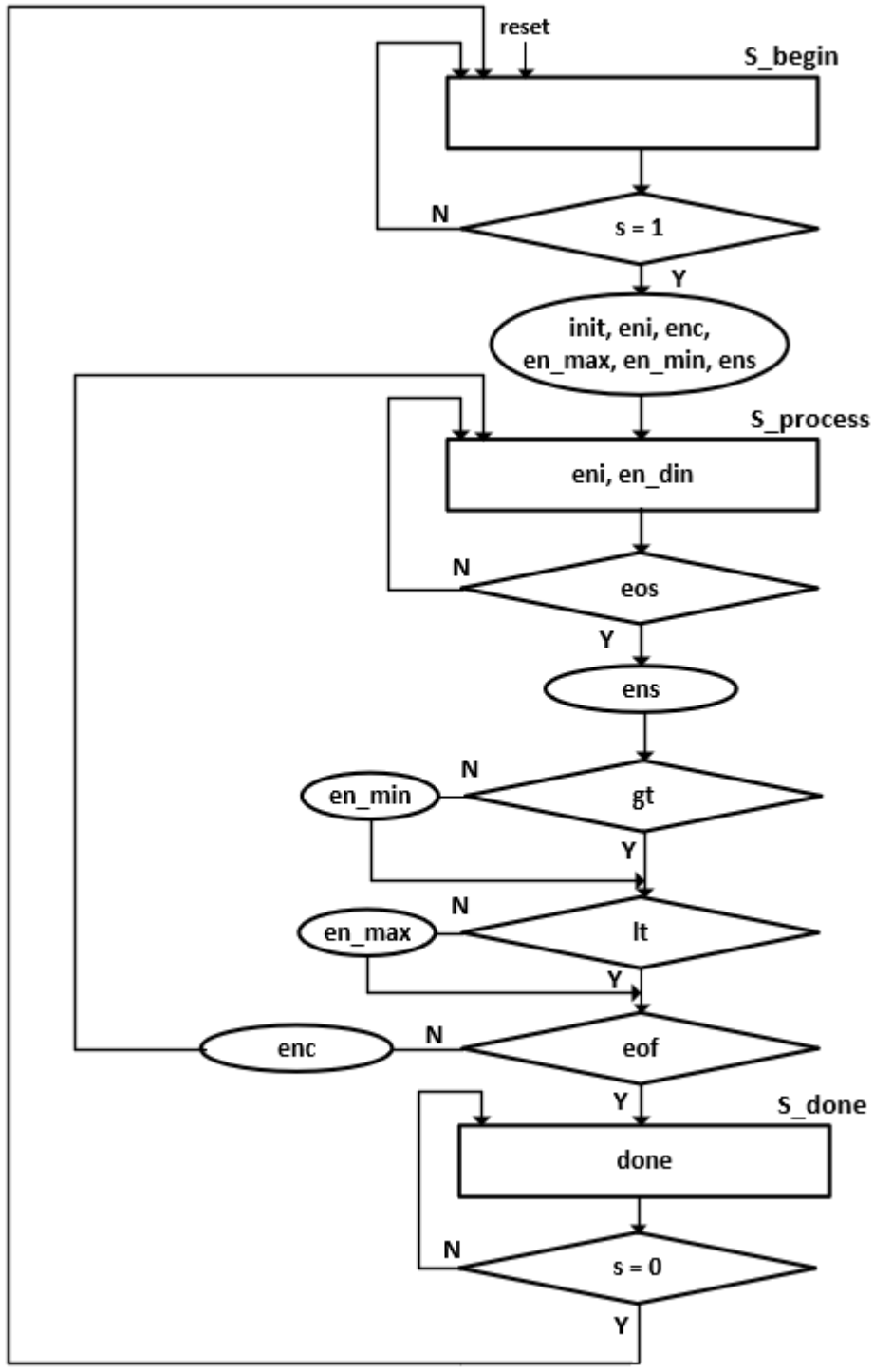
Table of input/output ports

Port	Width	Meaning
clk	1	System Clock
reset	1	System reset – clears all internal registers and counters. Active high.
din	8	Input data bus.
s	1	Operating mode: 0 = waiting for data/reading results 1 = processing
dout	m	One of the three results calculated by the circuit: avr (if sel_out=0), max (if sel_out=1), or min (if sel_out=2).
sel_out	2	Selection between the three calculated results: 0 = avr, 1 = max, 2 = min.
done	1	Asserted when all results are ready, zero otherwise.

Block diagram of the Datapath



ASM Chart


reset
S_begin
N
s = 1
Y
init, eni, enc,
en_max, en_min, ens
S_process
eni, en_din
N
eos
Y
ens
N
en_min
gt
Y
N
en_max
lt
Y
N
enc
eof
Y
S_done
done
N
s = 0
Y

Tasks:

Perform the following tasks:

1. Write a synthesizable VHDL code representing the circuit.
2. Write a testbench verifying the operation of your circuit for n=2 and m=8.
3. Perform functional simulation of your circuit and use it to debug your VHDL code. Take a printout of the waveform showing the entire operation.
4. Synthesize your circuit.
5. Implement your circuit using
    a. FPGA family: Artix-7
    b. Part name: XC7A35TCPG236-1
    c. Speed Grade: -1
6. Run the static timing analysis of your circuit. Determine the minimum clock period and the maximum clock frequency.
7. Based on the implementation reports, determine the number of CLB slices, LUTs, flip-flops, and pins used by the circuit.
8. Perform the timing simulation of your circuit at the maximum clock frequency returned by the static timing analysis. Take a printout of the waveform showing the entire operation.

Deliverables:

1. VHDL code of your entire circuit.
2. VHDL code of your testbench.
3. Timing waveforms from the functional and timing simulations demonstrating the correct operation of your circuit.
4. FPGA resource utilization (as defined in Task 7 above).
5. Minimum clock period and maximum clock frequency of your circuit.

ASCII TABLE

Decimal	Hex	Char	Decimal	Hex	Char	Decimal	Hex	Char	Decimal	Hex	Char
0	0	[NULL]	32	20	[SPACE]	64	40	@	96	60	`
1	1	[START OF HEADING]	33	21	!	65	41	A	97	61	a
2	2	[START OF TEXT]	34	22	"	66	42	B	98	62	b
3	3	[END OF TEXT]	35	23	#	67	43	C	99	63	c
4	4	[END OF TRANSMISSION]	36	24	$	68	44	D	100	64	d
5	5	[ENQUIRY]	37	25	%	69	45	E	101	65	e
6	6	[ACKNOWLEDGE]	38	26	&	70	46	F	102	66	f
7	7	[BELL]	39	27	'	71	47	G	103	67	g
8	8	[BACKSPACE]	40	28	(	72	48	H	104	68	h
9	9	[HORIZONTAL TAB]	41	29	)	73	49	I	105	69	i
10	A	[LINE FEED]	42	2A	*	74	4A	J	106	6A	j
11	B	[VERTICAL TAB]	43	2B	+	75	4B	K	107	6B	k
12	C	[FORM FEED]	44	2C	,	76	4C	L	108	6C	l
13	D	[CARRIAGE RETURN]	45	2D	-	77	4D	M	109	6D	m
14	E	[SHIFT OUT]	46	2E	.	78	4E	N	110	6E	n
15	F	[SHIFT IN]	47	2F	/	79	4F	O	111	6F	o
16	10	[DATA LINK ESCAPE]	48	30	0	80	50	P	112	70	p
17	11	[DEVICE CONTROL 1]	49	31	1	81	51	Q	113	71	q
18	12	[DEVICE CONTROL 2]	50	32	2	82	52	R	114	72	r
19	13	[DEVICE CONTROL 3]	51	33	3	83	53	S	115	73	s
20	14	[DEVICE CONTROL 4]	52	34	4	84	54	T	116	74	t
21	15	[NEGATIVE ACKNOWLEDGE]	53	35	5	85	55	U	117	75	u
22	16	[SYNCHRONOUS IDLE]	54	36	6	86	56	V	118	76	v
23	17	[ENG OF TRANS. BLOCK]	55	37	7	87	57	W	119	77	w
24	18	[CANCEL]	56	38	8	88	58	X	120	78	x
25	19	[END OF MEDIUM]	57	39	9	89	59	Y	121	79	y
26	1A	[SUBSTITUTE]	58	3A	:	90	5A	Z	122	7A	z
27	1B	[ESCAPE]	59	3B	;	91	5B	[	123	7B	{
28	1C	[FILE SEPARATOR]	60	3C	<	92	5C	\	124	7C	|
29	1D	[GROUP SEPARATOR]	61	3D	=	93	5D	]	125	7D	}
30	1E	[RECORD SEPARATOR]	62	3E	>	94	5E	^	126	7E	~
31	1F	[UNIT SEPARATOR]	63	3F	?	95	5F	_	127	7F	[DEL]