ECE 448

Final Exam

May 13, 2020

HONOR CODE PLEDGE: “On my honor I have neither given nor received aid on this exam”

Your first and last name (printed): …….

Your signature …….

Failure to sign the pledge may result in receiving no credit for the exam.

ECE 448
Spring 2020
Final Exam

Problem 0

Specify your Day of Birth Number, *dd*, and your Month of Birth Number, *mm*.

The day of month on which you were born is your Day of Birth Number.
The month of year when you were born is your Month of Birth Number.

These numbers are as follows:
Important Note: These numbers will be used only for the purpose of differentiating problems attempted by various students. However, if you do not feel comfortable revealing these numbers due to privacy concerns, you have the right to specify randomly chosen numbers that belong to a valid range.

dd **=** **[must be a number between 1 and 31]**

mm **=** **[must be a number between 1 and 12]**

In all following problems, please replace *dd* and *mm* by numerical values defined and specified above.

Problem 1

Calculate the maximum number of words *N* in the memory implemented using a 36-kbit Block RAM of Artix-7 FPGAs, assuming that the width of each word is given by the parameter *dd* specified in Problem 0.

Please provide the computations you performed.

Then, calculate the corresponding width of the address port of this memory, *r*.

Answer:

***N* =**

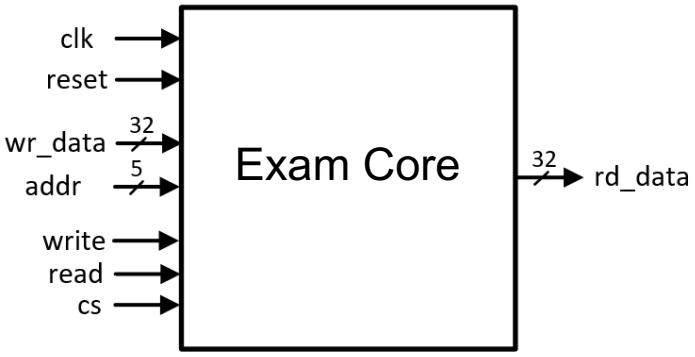
***r* =**

Justification:

Problem 2

Analyze the memory map and draw the detailed internal block diagram of an FPro MMIO Exam Core with the following interface and memory map shown on the next page.

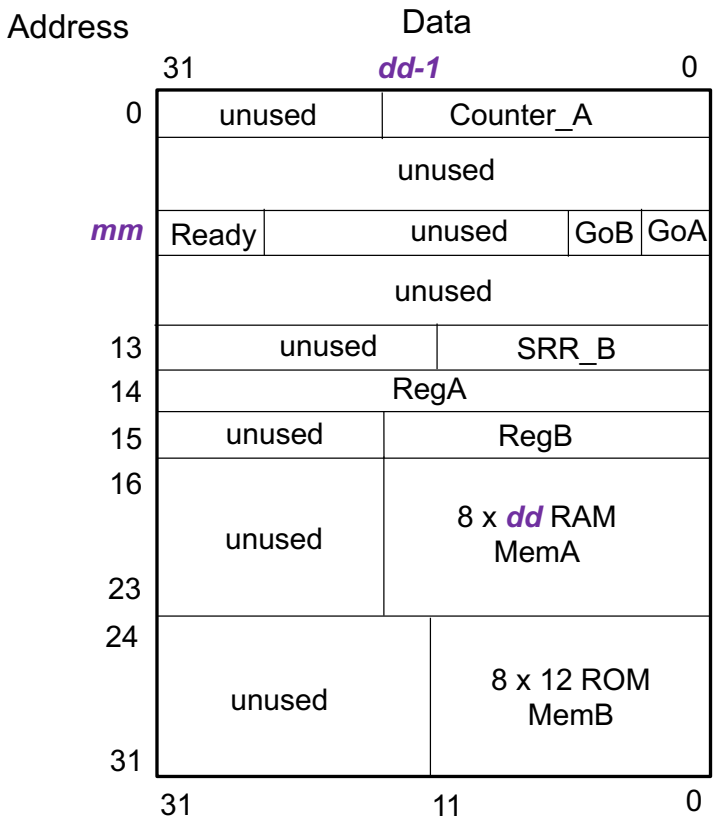
Interface:



Assumptions:

- **Parameters *dd* and *mm* should be replaced by the numerical values specified in Problem 0.**
- **Registers must be implemented using actual registers, not memory.**
- **RegA is a 32-bit read-only register.**
- **RegB can be written to and read from. This register has the width of *dd* bits.**
- **Counter_A is a *dd*-bit counter. Writing to a counter initializes this counter. Reading from a counter reads its current value. Assume that initializing a counter requires only an active value of the input Ld.**
- **SRR_B is a 12-bit shift register, shifting to the right , with parallel load, parallel output, serial input and serial output, and asynchronous reset active low. Assume that both Ld=1 and En = 1 are required to cause the parallel load. The processor should be able to initialize this shift register by writing to the address 13 and read its parallel output by reading from the same address.**
- **GoB and GoA are 1-bit write-only flags located at the two least significant bit locations (1 and 0, respectively) at the address *mm*.**
- **Ready is a 1-bit read-only flag located at the most significant bit location (31) at the address *mm*.**

Memory Map:



Solution to Problem 2:

Analysis of the Memory Map (recommended):

Block diagram (you can use an arbitrary number of pages):

Problem 3

A block diagram of the Homework 2 Datapath is given on the next page.

<u>Assume the following parameters of basic components:</u>

Delays of all registers and counters: $d_{REG} = 1$ ns

Setup time of all registers and counters: $t_{REG\text{-}setup} = 1$ ns

Reading delays of RAMs (from ADDR to DOUT): $d_{RAM\text{-}RD} = 4$ ns
(assume that all RAMs have asynchronous read)

Setup time of RAMs (between the signals at all inputs and the next rising edge of the clock):
$t_{RAM\text{-}setup} = 3$ ns

Delay of a fixed shifter to the right by 8 locations: $d_{FSR8} = 0$ ns

Delay of a 2-to-1 MUX: $d_{MUX2} = 3$ ns

Delay of a 3-to-1 MUX: $d_{MUX3} = 5$ ns

Delay of a *k*-bit adder (where *k* is the width of the widest input):

$$d_{ADD}(k) = \lceil \boldsymbol{mm}/4 \rceil + 0.5 \cdot (k - 2)$$

Delay of a *k*-bit subtractor (where *k* is the width of the widest input):

$$d_{SUB}(k) = \lceil \boldsymbol{mm}/4 \rceil + 0.5 \cdot (k - 2)$$

Delay of a *k*-bit comparator (where *k* is the width of the widest input):

$$d_{CMP}(k) = \lceil \boldsymbol{mm}/4 \rceil + 0.5 \cdot (k - 2)$$

<u>Assume that:</u>

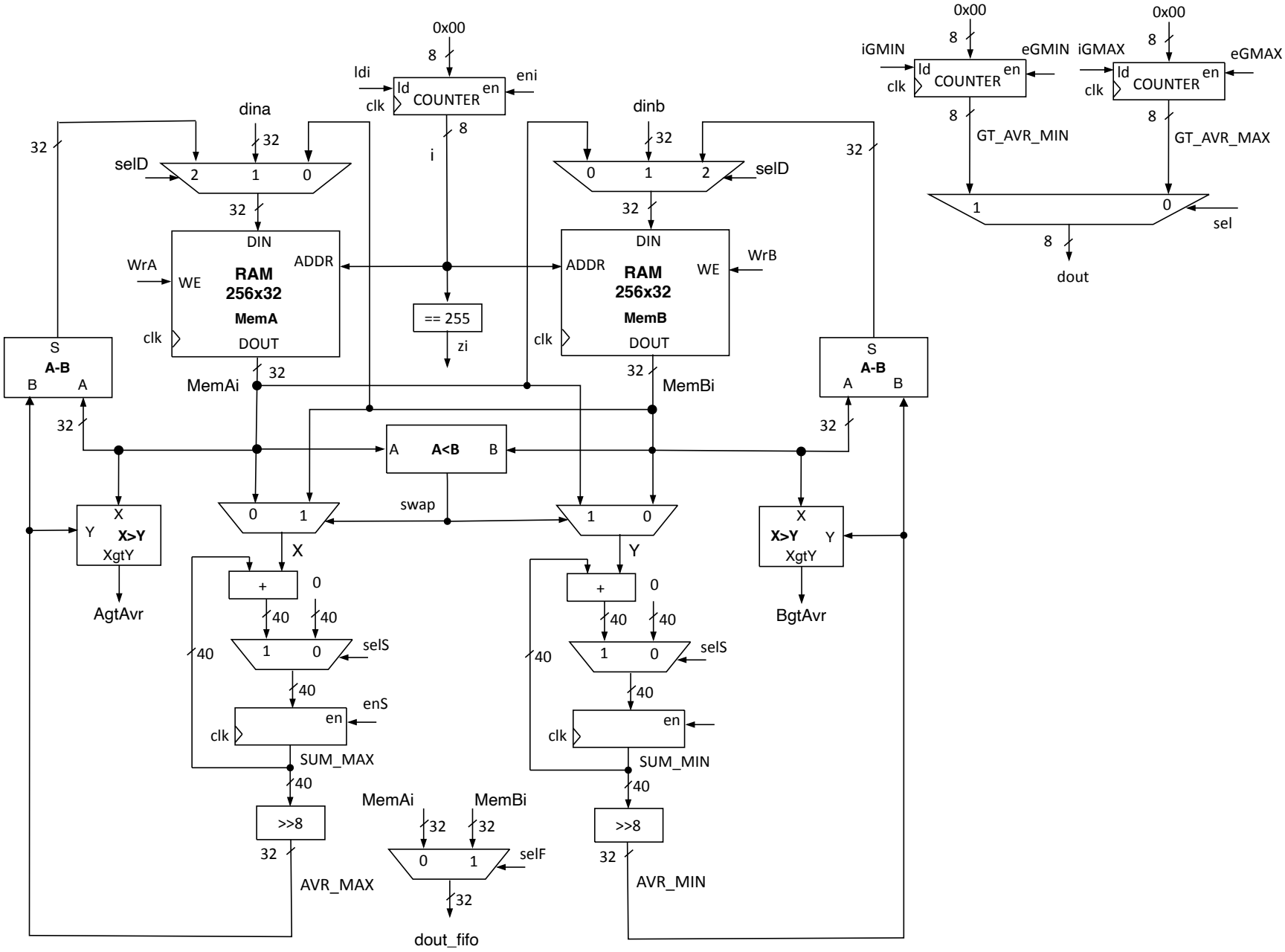
- ***mm*** should be replaced by the numerical value specified in Problem 0.
- The critical path is located entirely in the Datapath. Any paths involving delays of logic components of the Controller have shorter delays. Any paths involving delays of logic components of any external circuit have shorter delays.

Tasks:

Determine the critical path of this circuit and express it in terms of a sum of variables representing delays and setup times of all major components.

Calculate:

1. Critical path delay
2. Minimum clock period
3. Maximum clock frequency
4. Slack for the target clock frequency equal to 30 MHz.


0x00
8
ldi
ld
clk
COUNTER
en
eni
i
dina
dinb
32
selD
2 1 0
0 1 2
DIN
ADDR
WrA
WE
RAM
256x32
MemA
MemB
WrB
clk
DOUT
== 255
zi
MemAi
MemBi
S
A-B
B A
A B
A A<B B
swap
0 1
1 0
X
Y
X>Y
XgtY
AgtAvr
BgtAvr
+
40
1 0
selS
enS
SUM_MAX
SUM_MIN
>>8
AVR_MAX
AVR_MIN
selF
dout_fifo
iGMIN
eGMIN
iGMAX
eGMAX
GT_AVR_MIN
GT_AVR_MAX
sel
dout

Solution to Problem 3:

Formula for the critical path delay in terms of a sum of variables representing delays and setup times of all major components (including any calculations and justifications):

Critical path delay:

Minimum clock period:

Maximum clock frequency:

Slack for the target clock frequency equal to 30 MHz:

Problem 4

The Exam circuit is described below using its:

A. pseudocode
B. table of input/output ports.

Pseudocode:

MEM represents a dual-port memory of the size 512 x 8. This memory is initialized using a burst mode with the burst size equal to 512. The beginnings of the bursts are indicated with active value of the input `burst`. The start of calculations is indicated with the active value of the input `s`. The results are written to an output FIFO, as long as this FIFO is not full.

```
begin:
done = 0

wait for burst=1
for I = 0 to 511 do
   MEM[I] = din
end for

wait for s=1
MUL = 1

for J = 0 to ⌈mm/2⌉ do
    for IA = 0 to (256/2^J) - 1 do
           IB = (512/2^J)-IA-1
           if (MEM[IA] ≥ MEM[IB]) then
               X =  MEM[IA]
               Y =  MEM[IB]
               MEM[IA] = Y
               MEM[IB] = X
           end if
           if X ≠ 0 then
                MUL = MUL * X
                MUL = MUL mod 2^8   // equivalent to MUL = MUL7..0
           end if
    end for
end for

for I = 0 to 511 do
   wait for fifo_full = 0
   write MEM[I] to fifo
end for

done = 1
wait for s=0
go to begin
```

Please clearly mark the widths of all buses in your circuit.
mm should be replaced by the numerical value specified in Problem 0.

Assume the following interface to your circuit:

Port	Dir	Width	Meaning
clk	In	1	System clock.
reset	In	1	System reset. Active high.
s	In	1	Operating mode: 0 = initialization/reading results, 1 = processing.
din	In	8	Input data bus
burst	In	1	Start of the burst at the input dina
dout_fifo	Out	8	Output data bus connected to an external FIFO
wr_fifo	Out	1	Writing data to an external fifo
fifo_full	In	1	External FIFO full
done	Out	1	Asserted when all results are ready, zero otherwise

Perform the following tasks:

Task 1

Draw a block diagram of the datapath unit of the Exam circuit.

Task 2

Draw an interface of the Exam circuit, with the division into the Datapath and Controller.

Task 3

Draw an ASM chart describing the Controller of the Exam circuit using actions and expressions corresponding (as much as practical) to the operations and conditions of the pseudocode.

Task 4

Draw a second version of the same ASM chart, expressing

a. operations in terms of active values of control signals generated by the Controller.
b. conditions in terms of values of status signals generated by the Datapath.

Solution to Problem 4:

Analysis of variables (recommended):

Block diagram (you can use an arbitrary number of pages):

Interface with the division into the Datapath and Controller:

ASM chart based on the pseudocode:

ASM chart based on active values of control and status signals:

Problem 5

Based on the given below block diagram of the Text Generation Circuit with Tile Memory, please provide the following information:

A. Range of locations in the font ROM used to represent a font pattern of <u>the first character of your first name</u>:

B. Address of the location holding ASCII code of the tile with the coordinates x=*dd*, y=*mm*, where *dd* and *mm* are numerical values specified in Problem 0: