

Your First Name:  
Your Last Name:

ECE 448  
Midterm Exam  
Monday, March 2, 2020

**Problem 1**

Perform the following tasks for

**a combinational Variable Logical Shifter Right,**  
with the block diagram shown in Fig. 1.

A. Fill in the blanks in the code of this component given on the next page.

B. Draw a symbol of this component with the correct

- number
- direction, and
- widths

of ALL inputs and outputs.

Name each input and output, matching the VHDL code on the next page.

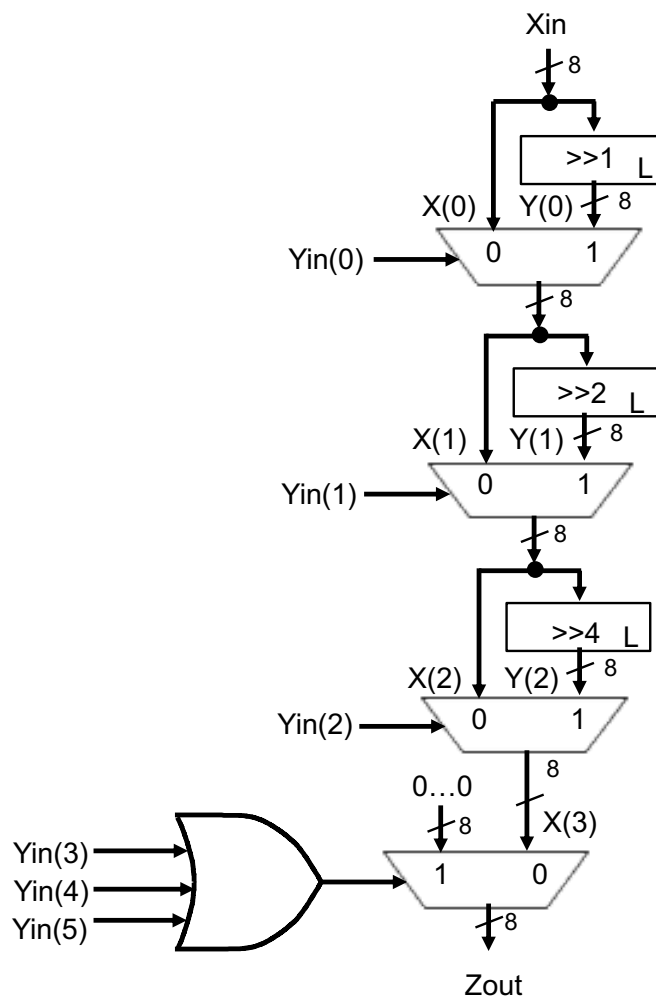


Fig. 1: Block diagram of a combinational Variable Logical Shifter Right

**Answer A:**

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;

ENTITY fixed_shifter_right IS
    ..... (L : INTEGER := 1);
    ..... (
        a : IN STD_LOGIC_VECTOR(7 downto 0);
        y : OUT STD_LOGIC_VECTOR(7 downto 0)
    );
END fixed_shifter_right;

ARCHITECTURE dataflow OF fixed_shifter_right IS
BEGIN
    y(7-L downto 0) <= .....;
    y(7 downto 7-L+1) <= .....;
END dataflow;

library IEEE;
use IEEE.STD_LOGIC_1164.all;

ENTITY variable_shifter_right IS
    PORT(
        Xin : IN STD_LOGIC_VECTOR(..... downto 0);
        Yin : IN STD_LOGIC_VECTOR(..... downto 0);
        Zout : OUT STD_LOGIC_VECTOR(..... downto 0)
    );
END variable_shifter_right;

ARCHITECTURE mixed OF variable_shifter_right IS

TYPE array8 IS ARRAY (0 to 3) OF .....;

SIGNAL X : array8;
SIGNAL Y : array8;

BEGIN
    X(0) <= .....;
    G: FOR i IN ..... TO ..... GENERATE

        SHIFT_I: ENTITY work.fixed_shifter_right(dataflow)
            GENERIC MAP (.....)
            PORT MAP ( ..... ,
                .....);

        X(i+1) <= ..... WHEN ..... ELSE .....;

    END GENERATE;
```

```

Zout <= ..... WHEN ..... ELSE
.....;

```

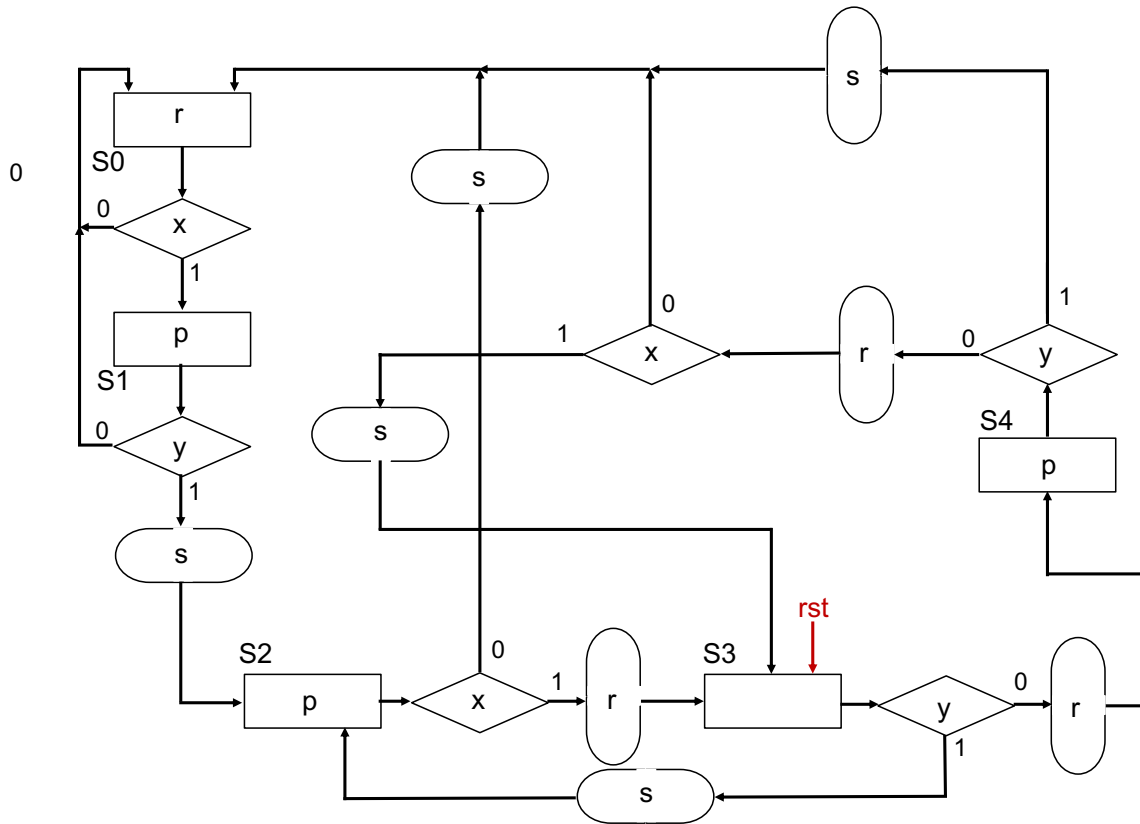
END mixed;

**Answer B:**

**Problem 2**

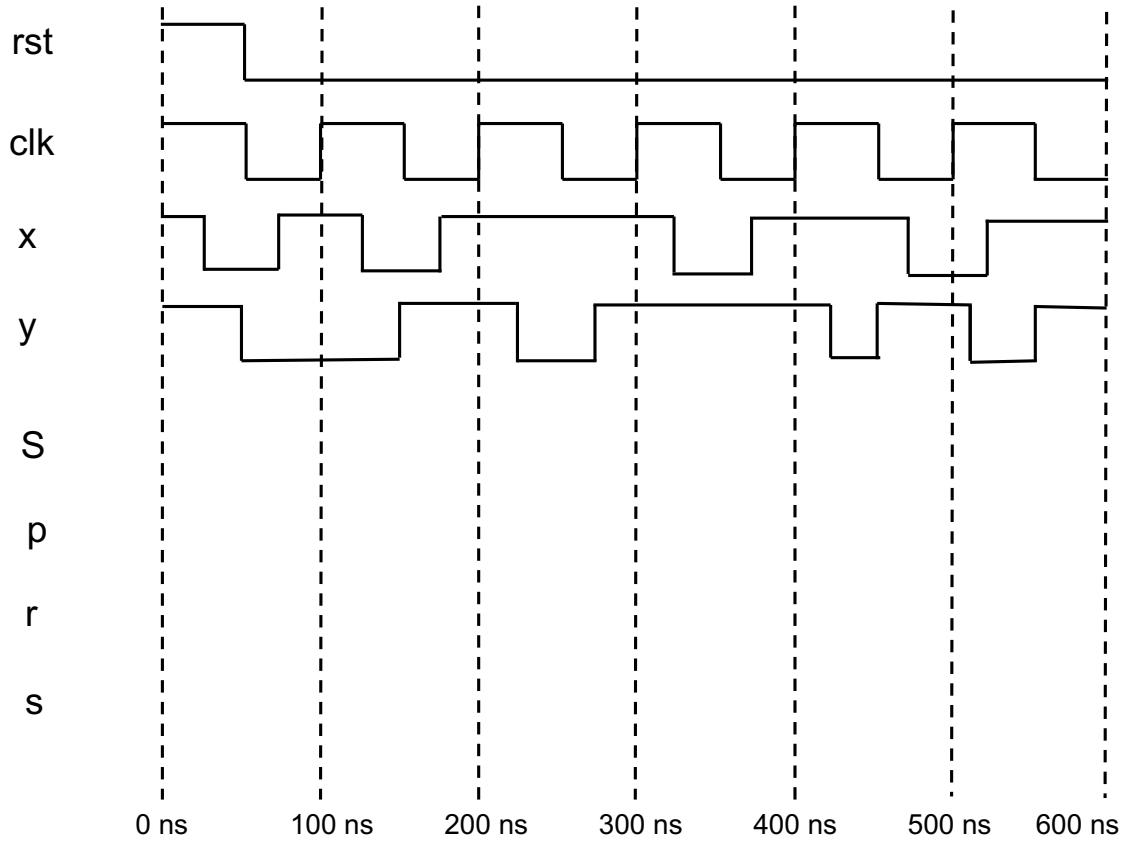
Assuming the controller described using the given below ASM chart:

- A. Supplement timing waveforms given on the next page with the values of the **state S**, and the values of the **outputs p, r, and s**.
- B. Fill in the blanks in the fragment of the code of this component given on the next page.



**Answer A:**

**Be careful regarding the initial value of the state S after reset!**



**Answer B:**

```
ARCHITECTURE behavioral of Controller IS
TYPE state IS (.....);
SIGNAL state_reg, state_next: .....;

BEGIN
P1: PROCESS (.....)
BEGIN
    IF(rst = '1') THEN
        state_reg <= .....;
    ELSIF rising_edge(clk) THEN
        state_reg <= .....;
    END IF;
END PROCESS;

Next_State_Output:
PROCESS (.....)
BEGIN
    .....;
    .....;
    .....;
    .....;
```

```
CASE state_reg IS
```

```
    WHEN S2 =>
```

```
    WHEN S3 =>
```

**Please provide the code only for the cases when state\_reg = S2 and state\_reg = S3.**

### **Problem 3**

Perform the following tasks for a component

**taking a 4-bit input A of the type std\_logic\_vector,  
adding to it a constant, given by the generic C of the type natural (in the  
range 0 to 15), and returning the sum S of the type std\_logic\_vector and the  
carry out Cout of the type std\_logic.**

- A. Draw a symbol of this component with the correct
  - number
  - direction, and
  - widthsof ALL inputs and outputs.  
Name each input and output.
- B. Write the full synthesizable code of this design entity, including entity declaration and architecture body, using the package numeric\_std.
- C. **(bonus)** Draw an internal block diagram of this component, composed of medium logic components and/or basic logic gates for the case of C=6.

**Answer A:**

**Answer B:**

You can use the following table of overloaded operators in the IEEE numeric\_std package

overloaded operator	description	data type of operand a	data type of operand b	data type of result
abs a - a	absolute value negation	signed		signed
a * b a / b a mod b a rem b a + b a - b	arithmetic operation	unsigned unsigned, natural signed signed, integer	unsigned, natural unsigned signed, integer signed	unsigned unsigned signed signed
a = b a /= b a < b a <= b a > b a >= b	relational operation	unsigned unsigned, natural signed signed, integer	unsigned, natural unsigned signed, integer signed	boolean boolean boolean boolean

**Answer C:**

