ECE 448
Midterm Exam
Monday, March 8, 2021

You do not have to print these questions!
You can provide all solutions by writing and drawing on blank pages!

Problem 1

Perform the following tasks for a 1-stage BCD adder defined as follows:

Inputs:
A, B: 4-bit wide inputs of the type std_logic_vector
Representing digits 0..9.
Cin: 1-bit input of the type std_logic
Outputs:
S : 4-bit wide output of the type std_logic_vector
Cout: 1-bit output of the type std_logic
Functionality:
S = A + B + Cin if (A + B + Cin) < 10
S = A + B + Cin – 10 otherwise
Cout = 1 if A + B + Cin >= 10
Cout = 0 otherwise

A. Draw a symbol of this component with the correct
- number
- direction, and
- widths

of ALL inputs and outputs.
Name each input and output.
B. Write the full synthesizable code of this design entity, including entity declaration and architecture body, using the package numeric_std.
C. Write the full structural description of a 3-digit BCD adder using the VHDL-93 convention for entity instantiation, including entity declaration and architecture body.

Hint: You can use the following table of overloaded operators in the IEEE numeric_std package

overloaded operator	description	data type of operand a	data type of operand b	data type of result
abs a - a	absolute value negation	signed		signed
a * b a / b a **mod** b a **rem** b a + b a - b	arithmetic operation	unsigned unsigned, natural signed signed, integer	unsigned, natural unsigned signed, integer signed	unsigned unsigned signed signed
a = b a /= b a < b a <= b a > b a >= b	relational operation	unsigned unsigned, natural signed signed, integer	unsigned, natural unsigned signed, integer signed	boolean boolean boolean boolean

Problem 2

A. Draw an internal block diagram of the logic component corresponding to the following VHDL code, assuming that you can use only <u>multiplexers and concatenations</u>. What is a proper name of this logic component (QA is not a valid answer)?

```
LIBRARY ieee;
USE ieee.std_logic_1164.all ;
ENTITY QA IS PORT (w : IN STD_LOGIC_VECTOR(1 DOWNTO 0);
                   En : IN STD_LOGIC ;
                   y : OUT STD_LOGIC_VECTOR(3 DOWNTO 0));
END QA;

ARCHITECTURE dataflow OF QA IS
SIGNAL Enw : STD_LOGIC_VECTOR(2 DOWNTO 0) ;
BEGIN
Enw <= En & w ;
WITH Enw SELECT
       y <= "0001" WHEN "100",
            "0010" WHEN "101",
            "0100" WHEN "110",
            "1000" WHEN "111",
            "0000" WHEN OTHERS ;
END dataflow ;
```

B. Draw an internal block diagram of the logic component corresponding to the following VHDL code, assuming that you can use only multiplexers and a single logic gate. What is a proper name of this logic component (QB is not a valid answer)?

```
LIBRARY ieee ;
USE ieee.std_logic_1164.all ;
ENTITY QB IS
      PORT (w : IN STD_LOGIC_VECTOR(3 DOWNTO 0);
            y : OUT STD_LOGIC_VECTOR(1 DOWNTO 0);
            z : OUT STD_LOGIC);
END QB ;

ARCHITECTURE dataflow OF QB IS
BEGIN
      y <=  "11" WHEN w(3) = '1' ELSE
            "10" WHEN w(2) = '1' ELSE
            "01" WHEN w(1) = '1' ELSE
            "00" ;
      z <= '0' WHEN w = "0000" ELSE '1';
END dataflow ;
```

C. Draw an internal block diagram of the logic component corresponding to the following VHDL code, assuming that you can use only registers and combinational incrementers. What is a proper name of this logic component?

```
LIBRARY ieee;
USE ieee.std_logic_1164.all;
USE ieee.numeric_std.all;
ENTITY QC IS
      PORT (Clock, Resetn, Enable : IN STD_LOGIC;
            Q : OUT   STD_LOGIC_VECTOR (3 DOWNTO 0));
END QC ;

ARCHITECTURE behavioral OF QC IS
      SIGNAL Count : UNSIGNED (3 DOWNTO 0);
BEGIN
      PROCESS (Clock, Resetn)
      BEGIN
            IF Resetn = '0' THEN
                  Count <= "0000";
            ELSIF rising_edge(Clock) THEN
                  IF Enable = '1' THEN
                        Count <= Count + 1;
                  END IF;
            END IF ;
      END PROCESS ;
      Q <= std_logic_vector(Count);
END behavioral ;
```

Problem 3

Write the entire VHDL code (including entity declaration and architecture body) of the controller described using the following ASM chart.

Assume that the default value of the outputs s2 and s3 is '-' (don't care).