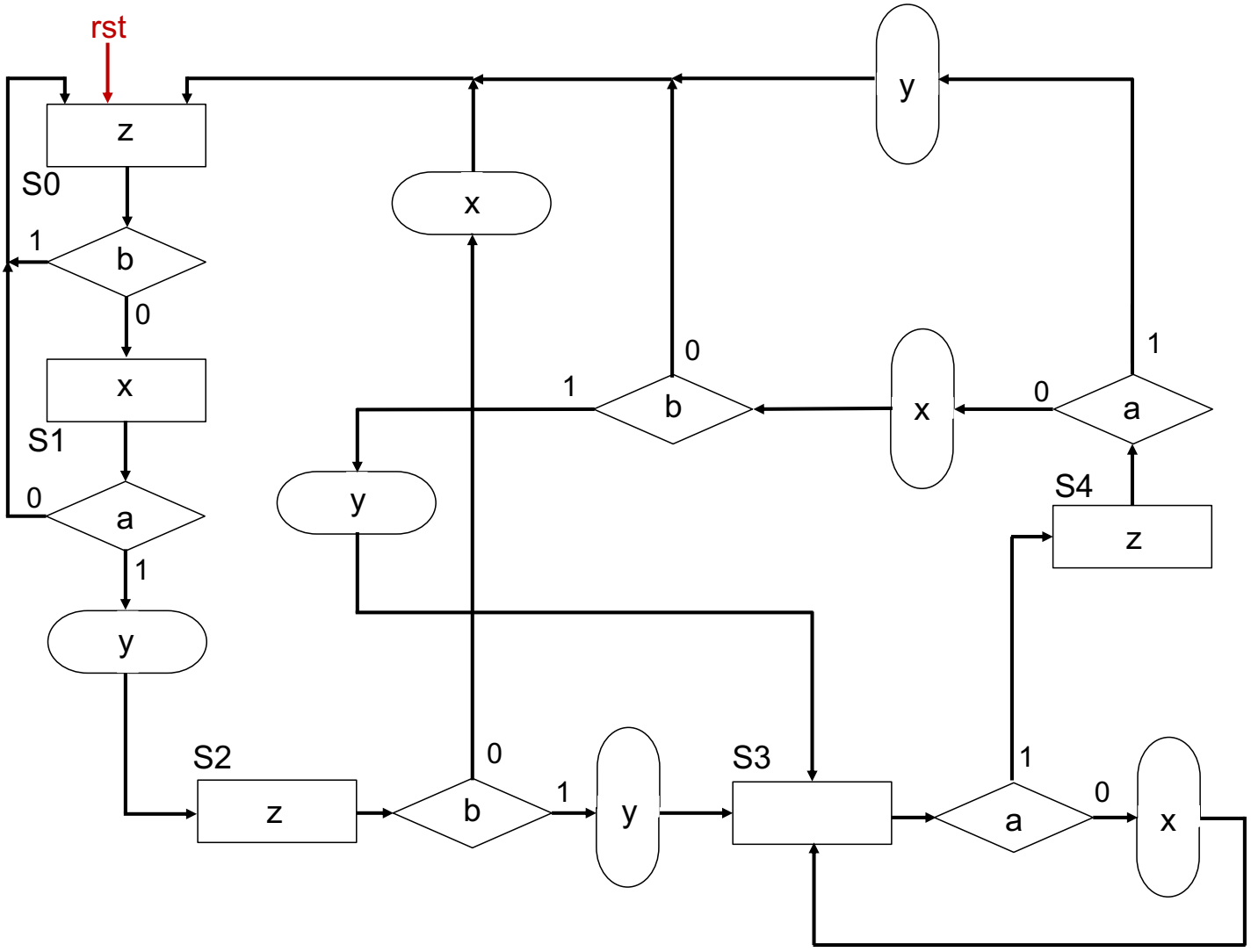
ECE 448
Midterm Exam
Thursday, March 2, 2023

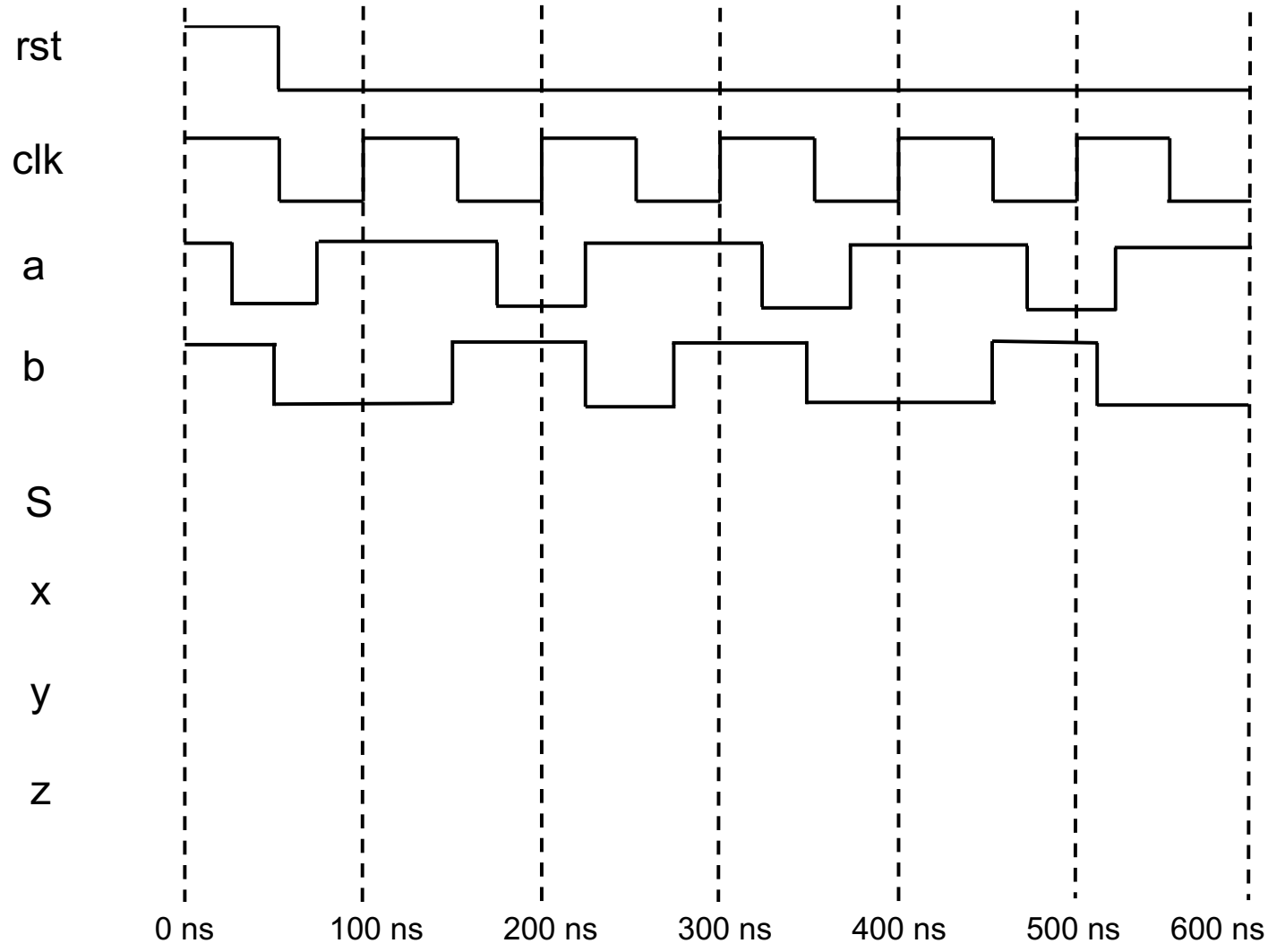
Problem 1

Assuming the controller described using the given below ASM chart:

A. Supplement timing waveforms given on the next page with the values of the **state S** and the values of the **outputs x**, **y**, and **z. Assume the use of asynchronous reset.**
B. Fill in the blanks in the fragment of the code of this component given on the next page.



Answer A:



Answer B:

```
ARCHITECTURE behavioral of Controller IS
TYPE state IS (……);
SIGNAL state_reg, state_next: ……;

BEGIN
P1: PROCESS(……)
BEGIN
      IF(rst = '1') THEN
            state_reg <= ……;
      ELSIF rising_edge(clk) THEN
            state_reg <= ……;
        END IF;
END PROCESS;
```

In the fragment below, provide the code only for the case when state_reg = S2.

```
Next_State_Output:
PROCESS (……)
BEGIN
      ……;
      ……;
      ……;
      ……;

      CASE state_reg IS

                  WHEN S2 =>
```

Problem 2

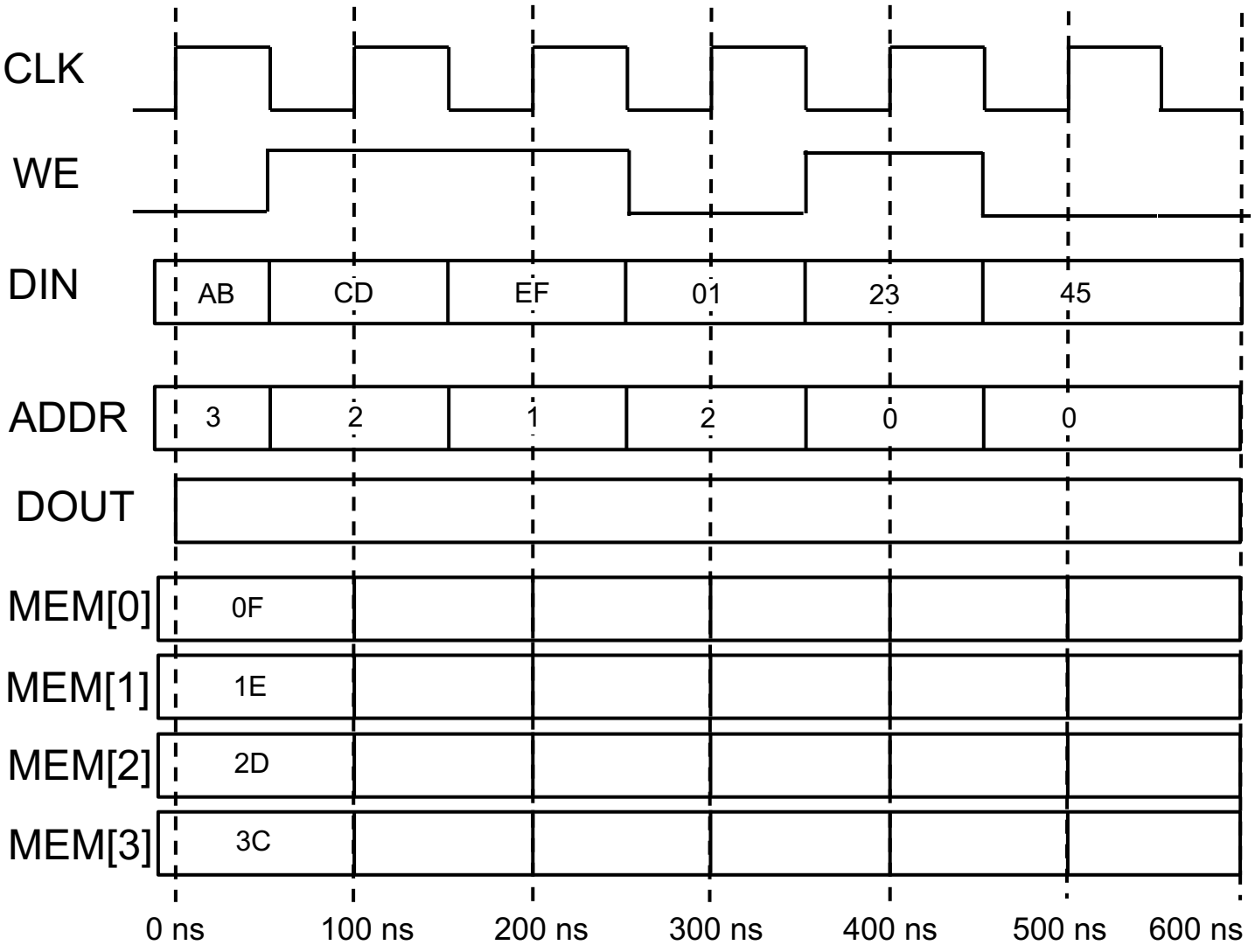
Draw a block diagram of the circuit given by the following VHDL code:

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use work.prng_pkg.all;

ENTITY PRNG IS
      PORT( Coeff             : in  std_logic_vector(4 downto 0);
            Load_Coeff        : in  std_logic;
            Seed              : in  std_logic_vector(4 downto 0);
            Init_Run          : in  std_logic;
            Clk               : in  std_logic;
            Current_State     : out std_logic_vector(4 downto 0));
END PRNG;


ARCHITECTURE mixed OF PRNG is
      signal Ands       : std_logic_vector(4 downto 0);
      signal Sin        : std_logic;
      signal Coeff_Q    : std_logic_vector(4 downto 0);
      signal Shift5_Q   : std_logic_vector(4 downto 0);

BEGIN
       -- Data Flow
      Sin <= Ands(0) XOR Ands(1) XOR Ands(2) XOR Ands(3) XOR Ands(4);
      Current_State <= Shift5_Q;
      Ands <= Coeff_Q AND Shift5_Q;

      -- Behavioral
      Coeff_Reg: PROCESS(Clk)
      BEGIN
            IF rising_edge(Clk)  THEN
                  IF Load_Coeff = '1'   THEN
                        Coeff_Q <= Coeff;
                  END IF;
            END IF;
      END PROCESS;

      -- Structural
      Shift5_Reg : ENTITY work.Shift5(behavioral) PORT MAP (D => Seed,
                                                            Load => Init_Run,
                                                            Sin => Sin,
                                                            Clock => Clk,
                                                            Q => Shift5_Q);
END mixed;
```

Answer:

Problem 3

Determine the value of the output DOUT and the contents of the 4x8 memory MEM for the following sequence of inputs and the given below initial contents of the memory MEM, **assuming zero delays** and the use of **RAM with asynchronous read**.
Assume that the values of DIN, ADDR, DOUT, MEM[0], MEM[1], MEM[2], and MEM[3] are provided and should be written in hexadecimal notation.



Problem 4

Show how to implement the following function using ROM:

$$Y = X^2 + 14,$$

where

A. X is a 3-bit unsigned integer.
B. X is a 3-bit signed integer.

Hint: Use as small as possible width of ROM words.

Required:

Draw a block diagram of your circuits and show the full contents of the ROM expressed in binary representation.

Answer for case A: X is a 3-bit unsigned integer:

Answer for case B: X is a 3-bit signed integer:

Bonus:

Write the VHDL code corresponding to case B, including the

- **library, package, and entity declarations**
- **architecture body,**

using the package numeric_std.

Answer 1 - assuming that your code explicitly uses and infers ROM

Answer 2 - assuming that your code uses a multiplication operator, *, of the numeric_std package.