## Resource Utilization after Synthesis:

| | | | | |
|---|---|---|---|---|
| Number of Slices: | 35 | out of | 960 | 3% |
| Number of Slice Flip Flops: | 37 | out of | 1920 | 1% |
| Number of 4 input LUTs: | 58 | out of | 1920 | 3% |
| Number of IOs: | 44 | | | |
| Number of bonded IOBs: | 41 | out of | 83 | 49% |
| Number of MULT18X18SIOs: | 1 | out of | 4 | 25% |
| Number of GCLKs: | 1 | out of | 24 | 4% |

## Resource Utilization after Implementation:

| | | |
|---|---|---|
| Number of External IOBs | 41 out of 83 | 49% |
| Number of External Input IOBs | 37 | |
| Number of External Input IBUFs | 37 | |
| Number of External Output IOBs | 4 | |
| Number of External Output IOBs | 4 | |
| Number of External Bidir IOBs | 0 | |
| Number of BUFGMUXs | 1 out of 24 | 4% |
| Number of MULT18X18SIOs | 1 out of 4 | 25% |
| Number of Slices | 40 out of 960 | 4% |
| Number of SLICEMs | 0 out of 480 | 0% |

## Timing and Critical path from Static timing analysis after PAR:

**Timing summary after Synthesis:**
Minimum period: 13.291ns (Maximum Frequency: 75.239MHz)

**Timing summary after Implementation:**
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Timing constraint: Default period analysis for net "clk_BUFGP"
658 paths analyzed, 37 endpoints analyzed, 0 failing endpoints
0 timing errors detected. (0 setup errors, 0 hold errors)
Minimum period is 7.071ns.
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Delay (setup path): 7.071ns (data path - clock path skew + uncertainty)
Source: Reg0/dout_8 (FF)
Destination: Shift0/qt_3 (FF)
Data Path Delay: 7.071ns (Levels of Logic = 5)
Clock Path Skew: 0.000ns
Source Clock: clk_BUFGP rising
Destination Clock: clk_BUFGP rising
Clock Uncertainty: 0.000ns

Maximum Data Path: Reg0/dout_8 to Shift0/qt_3

| Location | Delay type | Delay(ns) | Physical Resource<br>Logical Resource(s) |
|---|---|---|---|
| SLICE_X26Y8.XQ | Tcko | 0.592 | Reg0/dout<8><br>Reg0/dout_8 |
| SLICE_X22Y10.F2 | net (fanout=4) | 0.746 | Reg0/dout<8> |
| SLICE_X22Y10.X | Tilo | 0.759 | N15<br>Madd_add2_out_addsub0001_Madd_cy<0>11_SW0 |
| SLICE_X21Y9.G4 | net (fanout=1) | 0.348 | N15 |
| SLICE_X21Y9.Y | Tilo | 0.704 | Madd_add2_out_cy<1><br>Madd_add2_out_addsub0001_Madd_cy<0>11 |
| SLICE_X18Y8.F3 | net (fanout=7) | 0.373 | Madd_add2_out_addsub0001_Madd_cy<0> |
| SLICE_X18Y8.X | Tilo | 0.759 | N21<br>Madd_add2_out_xor<3>11_SW2_SW1 |
| SLICE_X19Y9.F2 | net (fanout=1) | 0.428 | N21 |
| SLICE_X19Y9.X | Tilo | 0.704 | N7<br>Madd_add2_out_xor<3>11_SW2 |
| SLICE_X13Y7.G1 | net (fanout=1) | 0.821 | N7 |
| SLICE_X13Y7.CLK | Tgck | 0.837 | Shift0/qt<3><br>Shift0/qt_mux0000<3>1<br>Shift0/qt_3 |
| Total | | 7.071ns (4.355ns logic, 2.716ns route)<br>(61.6% logic, 38.4% route) | |