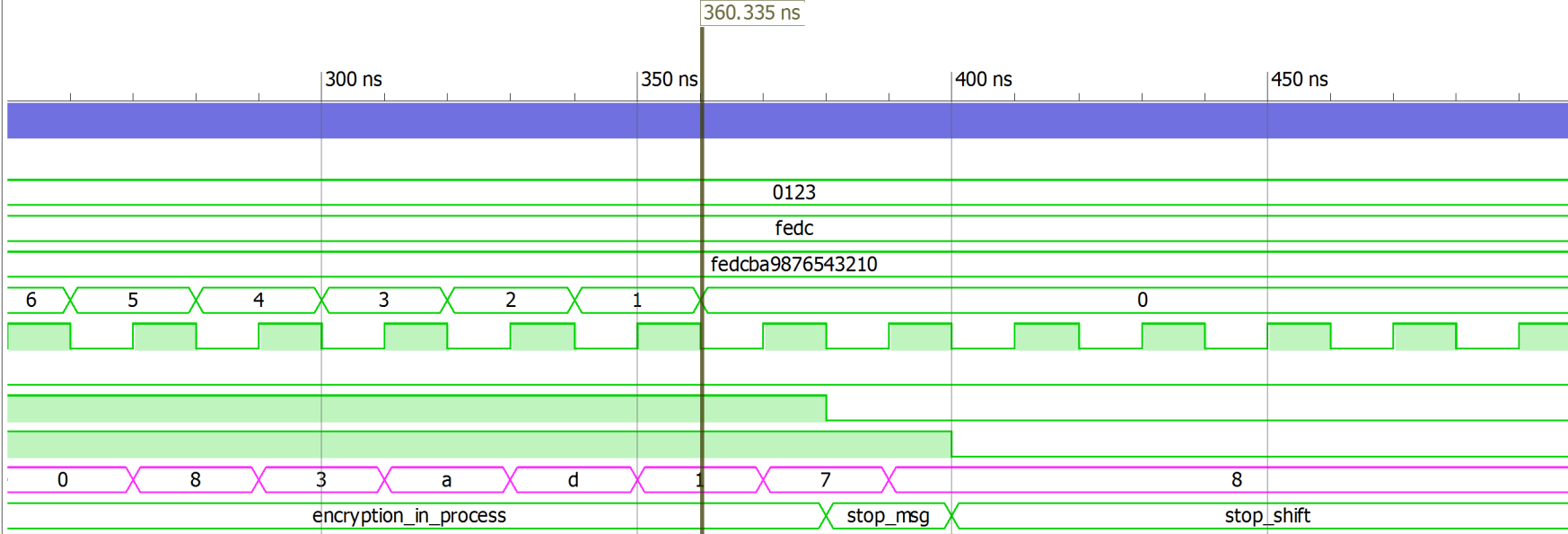


Testbench signals

- key[15:0]
- iv[15:0]
- msg_stream[63:0]
- msg[3:0]
- clk
- init
- run
- shift
- cph[3:0]
- state



UUT signals

- iv_shift_out[15:0]
- key_out[15:0]
- msg_out[3:0]
- xor1_out[3:0]
- xor2_out[3:0]
- add1_out[3:0]
- sub_out[3:0]
- rot2_out[3:0]
- shift3_out[3:0]
- mult_out[7:0]
- add2_out[3:0]
- cph_in[3:0]
- cph_out[3:0]
- cph[3:0]

