
110.072 ns
0 ns
20 ns
40 ns
60 ns
80 ns
100 ns
120 ns
Testbench signals
din[3:0]
zin[7:0]
clk
rst
state
init
en
cnz
en_cnt
count[2:0]
quotient_expected[3:0]
quotient_actual[3:0]
remainder_expected[3:0]
remainder_actual[3:0]
UUT signals
UUT signals
qi
cin
cout
en
en_cnt
count[2:0]
s[6:0]
d[3:0]
d_oc[3:0]
z[7:0]
mux_o[7:0]
sel_mux[1:0]
10
93
idle
processing
0
4
3
2
1
0
1001
0000
1101
1011
0110
1100
1001
0011
0000
0101
0001
0011
0110
0011
0
4
3
2
1
0
00
08
48
60
18
68
0
a
f
5
00
5d
1b
36
6c
39
01
5d
1b
36
6c
39
72
01
11
01
00
01
00