Report

Task 4: Critical path of the circuit

This listing is produced using Timing analyzer, after placing and routing, based on auto-generated timing constraints.

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Timing constraint: Default period analysis for net "clk_BUFGP"
107 paths analyzed, 41 endpoints analyzed, 0 failing endpoints
0 timing errors detected. (0 setup errors, 0 hold errors)
Minimum period is 3.234ns.

Delay (setup path):	3.234 ns (data path - clock path skew + uncertainty)
Source:	reg8/dout_sig_5 (FF)
Destination:	reg8/dout_sig_5 (FF)
Data Path Delay:	3.199ns (Levels of Logic = 3)
Clock Path Skew:	0.000ns
Source Clock:	clk_BUFGP rising
Destination Clock:	clk_BUFGP rising
Clock Uncertainty:	0.035ns

Clock Uncertainty:	0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ):	0.070ns
Total Input Jitter (TIJ):	0.000ns
Discrete Jitter (DJ):	0.000ns
Phase Error (PE):	0.000ns

Maximum Data Path at Slow Process Corner: reg8/dout_sig_5 to reg8/dout_sig_5

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
SLICE_X9Y4.CQ	Tcko	0.391	reg8/dout_sig<5> reg8/dout_sig_5
SLICE_X10Y4.D4	net (fanout=4)	0.794	reg8/dout_sig<5>
SLICE_X10Y4.D	Tilo	0.203	reg8/dout_sig<7> Mmux_mux_o<7:4>421
SLICE_X9Y4.D5	net (fanout=5)	0.406	Mmux_mux_o<7:4>42
SLICE_X9Y4.DMUX	Tilo	0.313	reg8/dout_sig<5> Mmux_mux_o<7:4>2_SW3
SLICE_X9Y4.C6	net (fanout=1)	0.770	N9
SLICE_X9Y4.CLK	Tas	0.322	reg8/dout_sig<5> Mmux_mux_o<7:4>2 reg8/dout_sig_5

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Total **3.199ns (1.229ns logic, 1.970ns route)**
(38.4% logic, 61.6% route)

Timing summary:

Timing errors: 0 Score: 0 (Setup/Max: 0, Hold: 0)

Constraints cover 176 paths, 0 nets, and 108 connections

Design statistics:
Minimum period: 3.234ns{1} (Maximum frequency: 309.215MHz)
Minimum input required time before clock: 2.288ns
Maximum output delay after clock: 7.224ns

Task 5: FPGA Resource Utilization After Implementation:

Number of occupied Slices:	**7**
Number of Slice LUTs:	**17**
Number of Slice Registers used as Flip-Flops:	**15**
Number of IO pins:	**23**

Slice Logic Utilization:

Number of Slice Registers:	**15 out of 18,224 1%**
Number used as Flip Flops:	**15**
Number used as Latches:	0
Number used as Latch-thrus:	0
Number used as AND/OR logics:	0
Number of Slice LUTs:	**17 out of 9,112 1%**
Number used as logic:	17 out of 9,112 1%
Number using O6 output only:	11
Number using O5 output only:	0
Number using O5 and O6:	6
Number used as ROM:	0
Number used as Memory:	0 out of 2,176 0%

Slice Logic Distribution:

Number of occupied Slices:	**7 out of 2,278 1%**
Number of MUXCYs used:	0 out of 4,556 0%

Number of LUT Flip Flop pairs used:	20
Number with an unused Flip Flop:	7 out of 20 35%
Number with an unused LUT:	3 out of 20 15%
Number of fully used LUT-FF pairs:	10 out of 20 50%
Number of slice register sites lost to control set restrictions:	0 out of 18,224 0%

IO Utilization:

Number of bonded IOBs:	**23 out of 232 9%**

Task 6: Minimum clock period and maximum clock frequency

Minimum period:	**3.234 ns**
Maximum frequency:	**309.215 MHz**