Report

Task 4: Critical path of the circuit

This information is extracted after placement and routing is done and using Timing analyzer in Xilinx ISE tool based on auto-generated timing constraints.

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Timing constraint: Default period analysis for net "clk_BUFGP"
8574 paths analyzed, 380 endpoints analyzed, 0 failing endpoints
0 timing errors detected. (0 setup errors, 0 hold errors)
Minimum period is **4.553ns**.

Delay (setup path):	4.553 ns (data path - clock path skew + uncertainty)
Source:	lfsr_2/Q_1 (FF)
Destination:	reg1/dout_sig_15 (FF)
Data Path Delay:	4.483ns (Levels of Logic = 3)
Clock Path Skew:	-0.035ns (0.268 - 0.303)
Source Clock:	clk_BUFGP rising
Destination Clock:	clk_BUFGP rising
Clock Uncertainty:	0.035ns

Clock Uncertainty:	0.035ns ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
Total System Jitter (TSJ):	0.070ns
Total Input Jitter (TIJ):	0.000ns
Discrete Jitter (DJ):	0.000ns
Phase Error (PE):	0.000ns

Maximum Data Path at Slow Process Corner: lfsr_2/Q_1 to reg1/dout_sig_15

Location	Delay type	Delay(ns)	Physical Resource Logical Resource(s)
SLICE_X3Y2.BQ	Tcko	0.391	lfsr_2/Q<1> lfsr_2/Q_1
SLICE_X3Y2.C2	net (fanout=14)	1.209	lfsr_2/Q<1>
SLICE_X3Y2.C	Tilo	0.259	lfsr_2/Q<1> Mmult_mult_out_Madd_51_SW0
SLICE_X4Y4.B6	net (fanout=1)	0.815	N3
SLICE_X4Y4.DMUX	Topbd	0.537	mult_out<7> Mmult_mult_out_Madd3_lut<5> Mmult_mult_out_Madd3_xor<7>
SLICE_X6Y7.B5	net (fanout=9)	0.689	mult_out<7>
SLICE_X6Y7.CLK	Tas	0.583	reg1/dout_sig<15> reg1/Maccum_dout_sig_lut<13>

reg1/Maccum_dout_sig_xor<15>
reg1/dout_sig_15

Total **4.483ns (1.770ns logic, 2.713ns route)**
(39.5% logic, 60.5% route)

Timing summary:

Timing errors: 0 Score: 0 (Setup/Max: 0, Hold: 0)

Constraints cover 8774 paths, 0 nets, and 423 connections

Design statistics:
Minimum period: 4.553ns{1} (Maximum frequency: 219.635MHz)
Minimum input required time before clock: 3.598ns
Maximum output delay after clock: 7.202ns

Task 5: FPGA Resource Utilization After Implementation:

Slice Logic Utilization:

Number of Slice Registers:	**84 out of 18,224 1%**
Number used as Flip Flops:	**84**
Number used as Latches:	0
Number used as Latch-thrus:	0
Number used as AND/OR logics:	0
Number of Slice LUTs:	**88 out of 9,112 1%**
Number used as logic:	82 out of 9,112 1%
Number using O6 output only:	54
Number using O5 output only:	0
Number using O5 and O6:	28
Number used as ROM:	0
Number used as Memory:	0 out of 2,176 0%
Number used exclusively as route-thrus:	6
Number with same-slice register load:	6
Number with same-slice carry load:	0
Number with other load:	0

Slice Logic Distribution:

Number of occupied Slices:	**28 out of 2,278 1%**
Number of MUXCYs used:	48 out of 4,556 1%
Number of LUT Flip Flop pairs used:	90
Number with an unused Flip Flop:	29 out of 90 32%
Number with an unused LUT:	2 out of 90 2%

Number of fully used LUT-FF pairs:	59 out of 90	65%
Number of slice register sites lost to control set restrictions:	0 out of 18,224	0%

Task 6: Minimum clock period and maximum clock frequency

Minimum period	:	**4.553ns**
Maximum frequency	:	**219.635MHz**