Resource Utilization after Synthesis:

Slice Logic Utilization:

Number of Slice Registers:	30	out of 18224	0%
Number of Slice LUTs:	33	out of 9112	0%
Number used as Logic:	33	out of 9112	0%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used:	36		
Number with an unused Flip Flop:	6	out of 36	16%
Number with an unused LUT:	3	out of 36	8%
Number of fully used LUT-FF pairs:	27	out of 36	75%
Number of unique control sets:	4		

IO Utilization:

Number of bonded IOBs:	10	out of 232	4%
Number of BUFG/BUFGCTRLs:	1	out of 16	6%

Resource Utilization after Implementation:

Slice Logic Utilization:

Number of Slice Registers:	30	out of 18,224	1%
Number of Slice LUTs:	30	out of 9,112	1%
Number used as logic:	30	out of 9,112	1%
Number of BUFG/BUFGMUXs:	1	out of 16	6%
Number of bonded IOBs:	10	out of 232	4%

Timing and Critical path from Static Timing Analysis:

Timing summary after Synthesis:

Minimum period: 2.954ns (Maximum Frequency: 338.570MHz)

Timing summary after Implementation:

Minimum period: 2.362ns{1} (Maximum frequency: 423.370MHz)

Critical Path:

```
==============================================================================
Timing constraint: Default period analysis for net "clk_BUFGP"
 235 paths analyzed, 112 endpoints analyzed, 0 failing endpoints
 0 timing errors detected. (0 setup errors, 0 hold errors)
 Minimum period is   2.362ns.
--------------------------------------------------------------------------------
Delay (setup path):       2.362  ns (data path - clock path skew + uncertainty)
  Source:               control_unit/y_FSM_FFd6    (FF)
  Destination:          datapath_unit/LFSR_gen[0].LFSRs/Q_1    (FF)
  Data Path Delay:      2.316ns (Levels of Logic = 2)
  Clock Path Skew:      -0.011ns (0.143 - 0.154)
  Source Clock:         clk_BUFGP rising
  Destination Clock:    clk_BUFGP rising
  Clock Uncertainty:    0.035ns

  Clock Uncertainty:          0.035ns  ((TSJ^2 + TIJ^2)^1/2 + DJ) / 2 + PE
    Total System Jitter (TSJ):  0.070ns
    Total Input Jitter (TIJ):   0.000ns
    Discrete Jitter (DJ):       0.000ns
    Phase Error (PE):           0.000ns

    Maximum Data Path at Slow Process Corner: control_unit/y_FSM_FFd6 to
datapath_unit/LFSR_gen[0].LFSRs/Q_1
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    SLICE_X12Y6.CQ       Tcko                  0.408   control_unit/y_FSM_FFd7
                                                       control_unit/y_FSM_FFd6
    SLICE_X14Y6.D3       net (fanout=3)        0.814   control_unit/y_FSM_FFd6
    SLICE_X14Y6.D        Tilo                  0.203   control_unit/y_FSM_FFd5
                                                       datapath_unit/en_lfsr<0>1
    SLICE_X12Y7.B6       net (fanout=4)        0.550   datapath_unit/en_lfsr<0>
    SLICE_X12Y7.CLK      Tas                   0.341   datapath_unit/LFSR_gen[0].LFSRs/Q<3>
                                                       datapath_unit/LFSR_gen[0].LFSRs/Q_1_rstpot
                                                       datapath_unit/LFSR_gen[0].LFSRs/Q_1
    -------------------------------------------------  ---------------------------
    Total                                      2.316ns (0.952ns logic, 1.364ns route)
                                                       (41.1% logic, 58.9% route)

--------------------------------------------------------------------------------
```