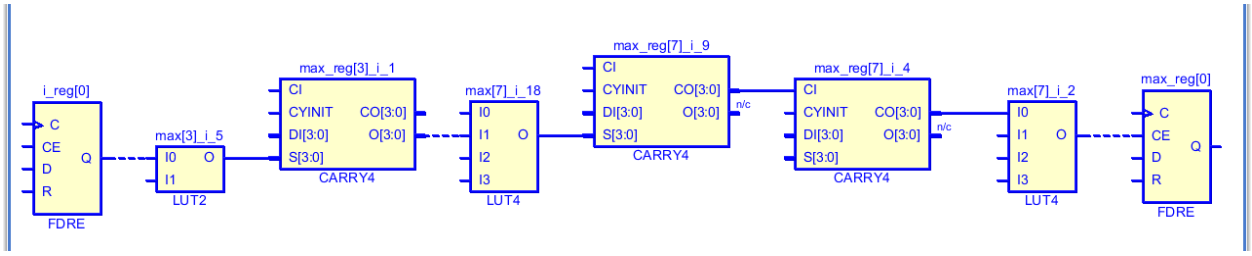
Reports | Design Runs | DRC | Methodology | Power | Timing

Design Timing Summary

		Hold		Pulse Width	
st Negative Slack (WNS):	4.090 ns	Worst Hold Slack (WHS):	0.226 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
ber of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Number of Endpoints:	118	Total Number of Endpoints:	118	Total Number of Endpoints:	52

$$Min\ period = current\ period - WNS = 10\ ns - 4.090\ ns = 5.910\ ns$$

$$Max_{clock} = \frac{1}{MinPeriod} = 169.2\ MHz$$



Path 1 - toplevel_timing_summary_routed

Summary

Name	Path 1
Slack	4.090ns
Source	i_reg[0]/C (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})
Destination	max_reg[0]/CE (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@5.000ns period=10.000ns})
Path Group	sys_clk_pin
Path Type	Setup (Max at Slow Process Corner)
Requirement	10.000ns (sys_clk_pin rise@10.000ns - sys_clk_pin rise@0.000ns)
Data Path Delay	5.643ns (logic 2.483ns (43.998%) route 3.160ns (56.002%))
Logic Levels	6 (CARRY4=3 LUT2=1 LUT4=2)
Clock Path Skew	-0.026ns
Clock Un...rtainty	0.035ns

Source Clock Path

Delay Type	Incr (ns)	Path ...	Location	Netlist Resource(s)
(clock sys_clk_pin rise edge)	(r) 0.000	0.000		
	(r) 0.000	0.000	Site: W5	clk
net (fo=0)	0.000	0.000		clk
IBUF (Prop_ibuf_I_O)	(r) 1.458	1.458	Site: W5	clk_IBUF_inst/O
net (fo=1, routed)	1.967	3.425		clk_IBUF
BUFG (Prop_bufg_I_O)	(r) 0.096	3.521	Site: BUF...TRL_X0Y0	clk_IBUF_BUFG_inst/O
net (fo=51, routed)	1.635	5.156		clk_IBUF_BUFG
FDRE			Site: SLICE_X5Y6	i_reg[0]/C

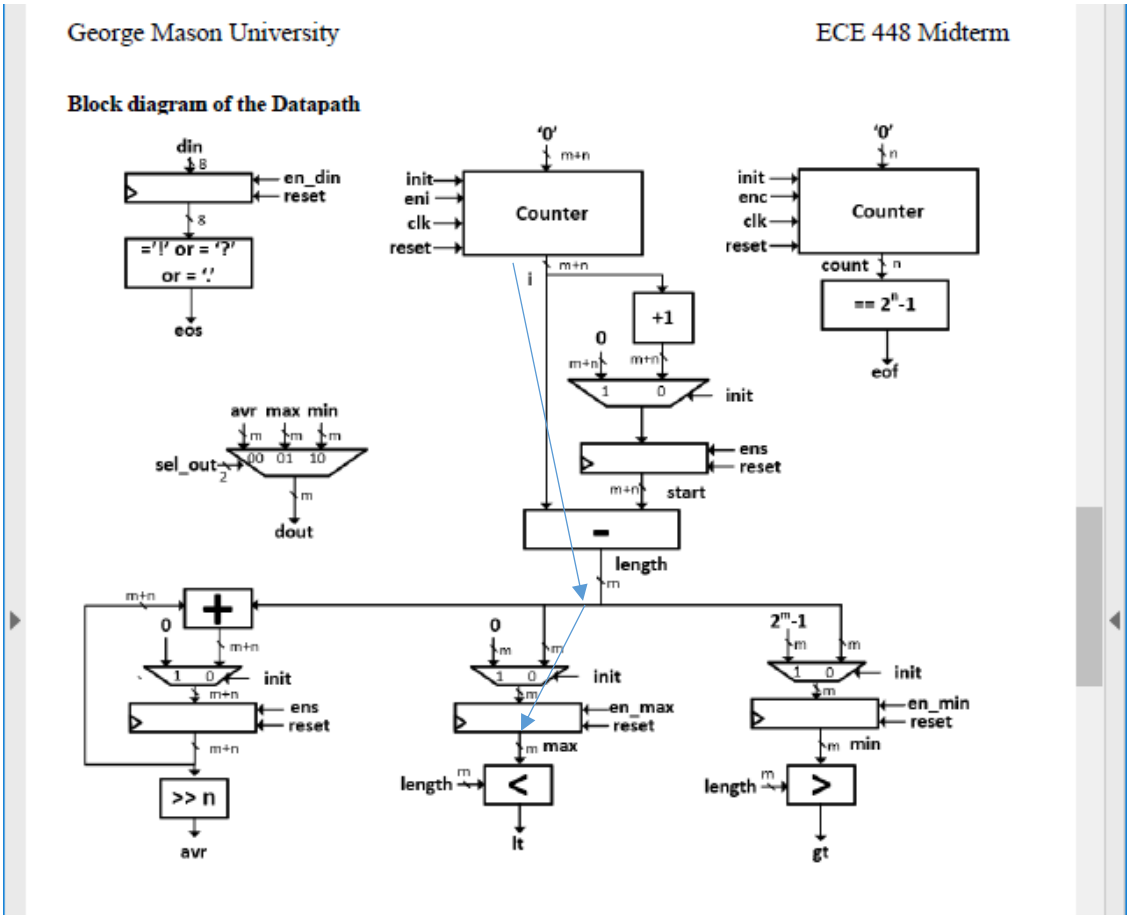
Data Path

Delay Type	Incr (ns)	Path (...	Location	Netlist Resource(s)
FDRE (Prop_fdre_C_Q)	(r) 0.456	5.612	Site: SLICE_X5Y6	i_reg[0]/Q
net (fo=9, routed)	0.797	6.409		i_reg_n_0_[0]
LUT2 (Prop_lut2_I0_O)	(r) 0.124	6.533	Site: SLICE_X4Y7	max[3]_i_5/O
net (fo=1, routed)	0.000	6.533		max[3]_i_5_n_0
CARRY4 (Prop_carry4_S[0]_O[1])	(r) 0.424	6.957	Site: SLICE_X4Y7	max_reg[3]_i_1/O[1]
net (fo=7, routed)	1.134	8.092		p_1_in[1]
LUT4 (Prop_lut4_I1_O)	(r) 0.303	8.395	Site: SLICE_X5Y8	max[7]_i_18/O
net (fo=1, routed)	0.000	8.395		max[7]_i_18_n_0
CARRY4 (Prop_c...4_S[0]_CO[3])	(r) 0.532	8.927	Site: SLICE_X5Y8	max_reg[7]_i_9/CO[3]
net (fo=1, routed)	0.000	8.927		max_reg[7]_i_9_n_0
CARRY4 (Prop_carry4_CI_CO[0])	(f) 0.271	9.198	Site: SLICE_X5Y9	max_reg[7]_i_4/CO[0]
net (fo=1, routed)	0.578	9.776		lt
LUT4 (Prop_lut4_I0_O)	(r) 0.373	10.149	Site: SLICE_X5Y7	max[7]_i_2/O
net (fo=8, routed)	0.651	10.800		en_max
FDRE			Site: SLICE_X4Y7	max_reg[0]/CE
Arrival Time		10.800		

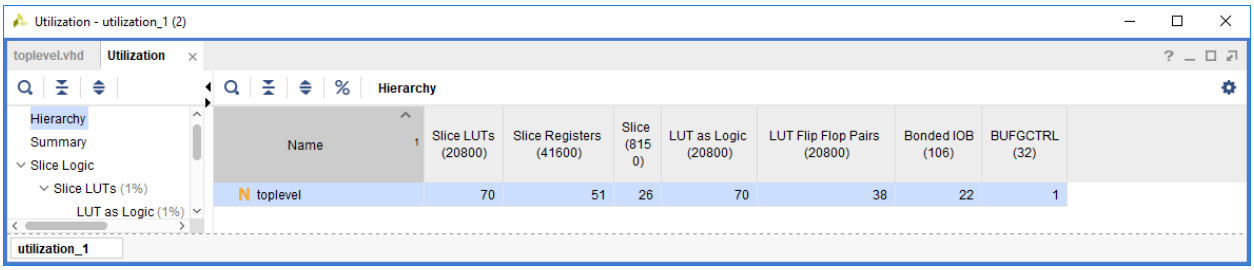
Destination Clock Path

Delay Type	Incr (ns)	Path (	Location	Netlist Resource(s)

Worst Path



Utilization



Slices : 26

LUTs : 70

FF : 51

Pins : 22