Midterm Exam ECE 448
Spring 2021
Tuesday, March 9
15 points

Instructions:
Zip all your deliverables into an archive <last_name>.zip and submit it through Blackboard no later than Tuesday, March 9, 11:40 AM EST.

Textual Description

A shift/subtract sequential restoring divider for unsigned integers performs the division z/d = q rem r, assuming $z_{2k-1..k} < d$, where z is a 2k-bit unsigned integer and d is a k-bit unsigned integer. The abbreviation rem stands for the remainder.

z, d, q, and r fulfill the following equations:

$$z = d \cdot q + r$$
$$r < d$$

For example, for k=4,

$$154 / 10 = 15 \text{ rem } 4$$

because

$$154 = 10 \cdot 15 + 4$$
and
$$4 < 10.$$

Please note that

$$154 = 10011010_2$$

Thus,

$$z_{7..4} = 9 < 10 = d.$$

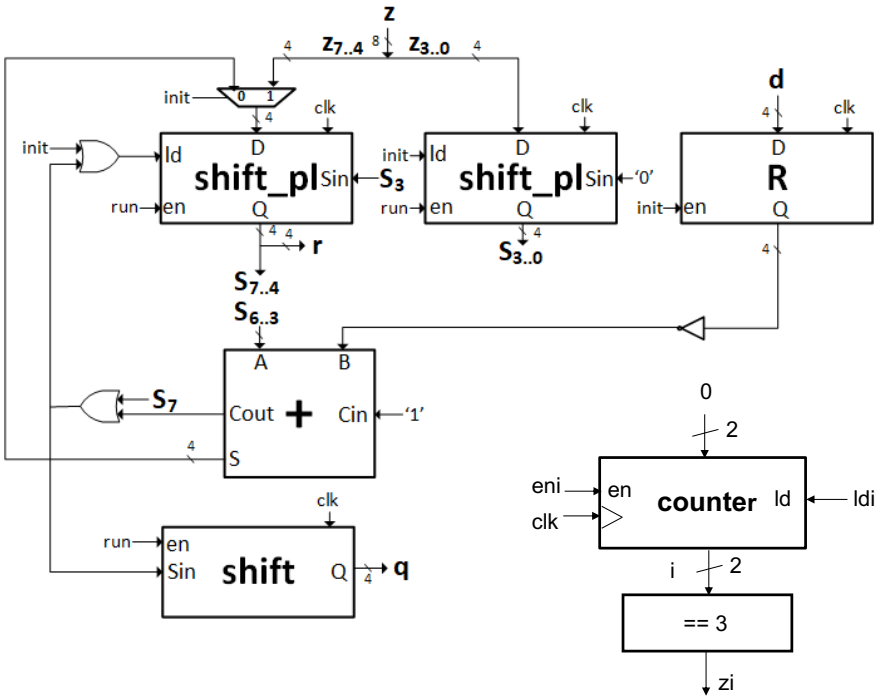
The circuit is specified below for k=4 using its:

- Table of input/output ports
- Block diagram of the Datapath
- Interface with the division into the Datapath and Controller
- ASM chart of the Controller.

Table of input/output ports

Port	Width	Meaning
clk	1	System clock.
reset	1	System reset. Active high.
z	8	Dividend.
d	4	Divisor.
q	4	Quotient.
r	4	Remainder.
Start	1	Control input indicating the start of calculations.
Done	1	Status output indicating that the results q and r are ready.

Block diagram of the Datapath

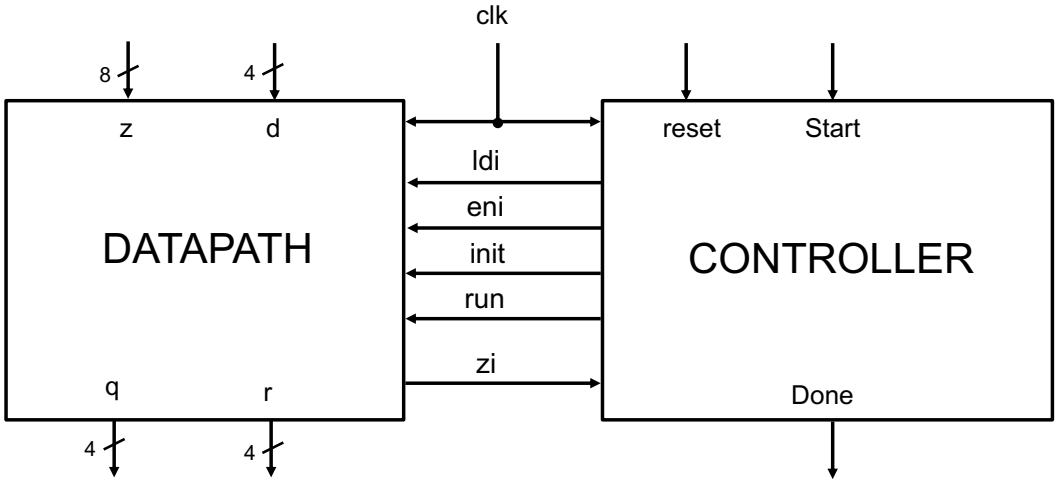


Notation:
shift_pl denotes a 4-bit shift register with parallel load, shifting to the left
shift denotes a 4-bit shift register, shifting to the **left**
R denotes a 4-bit register
+ denotes a 4-bit unsigned adder

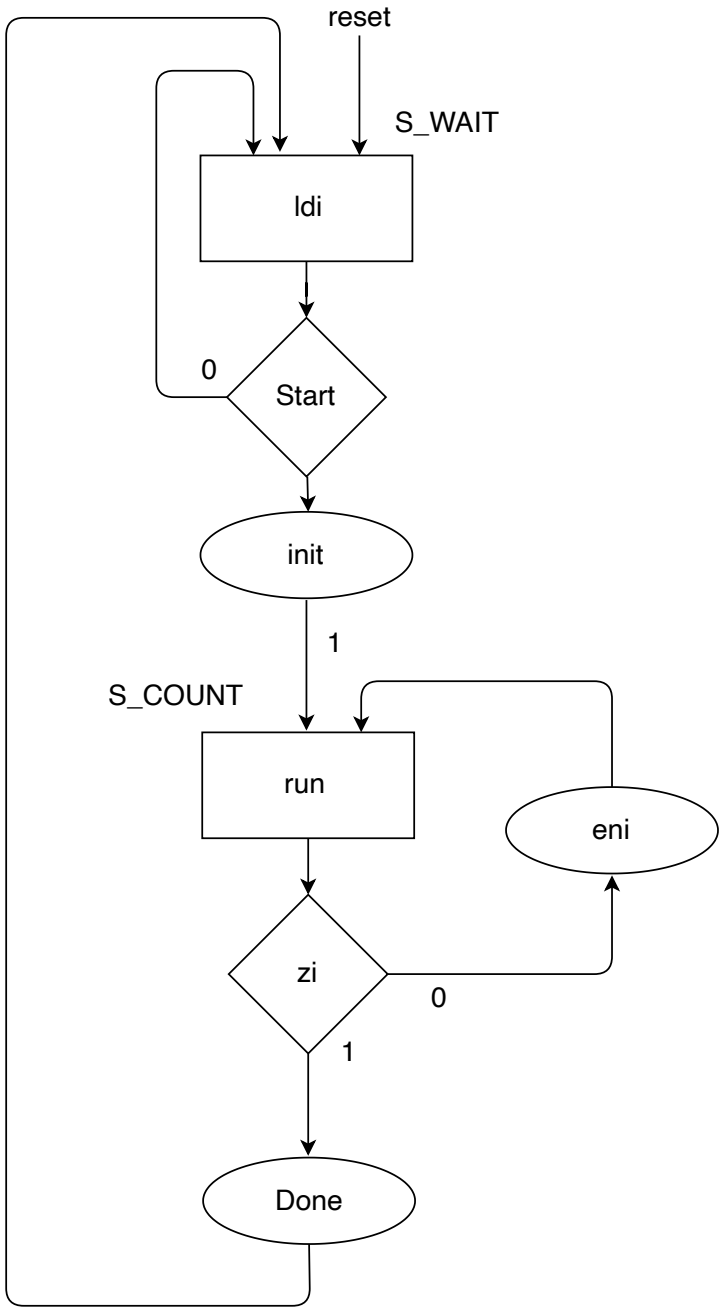
Assume:

Load inputs ld by themselves are sufficient to initialize all shift registers and counters!

Interface with the division into the Datapath and Controller:



ASM chart of the controller:



Required Tasks:

Perform the following tasks:

1. Write a synthesizable VHDL code representing the specified above circuit.
2. Write a testbench verifying the operation of your circuit for at least two values of z and d fulfilling the dependence $z_{7..4} < d$.
3. Perform functional simulation of your circuit and use it to debug your VHDL code. Take a printout of the waveforms showing the entire operation.
4. Synthesize your circuit.
5. Implement your circuit using
    a. FPGA family: Artix-7
    b. Part name: XC7A35TCPG236-1
    c. Speed Grade: -1
6. Based on the implementation reports, determine the number of CLB slices, LUTs, flip-flops, and pins used by the circuit.
7. Generalize your circuit by modifying its block diagram so it operates correctly for an arbitrary value of k.
8. Modify your code accordingly.
9. Demonstrate the correct operation of your modified code for k=4 and k=5.
10. Determine the resource utilization of your circuit for k=5 and k=16.

Deliverables:

1. VHDL code of your entire circuit for k=4.
2. VHDL code of your entire circuit for an arbitrary value of k.
3. VHDL code of your testbench, capable of verifying the operation of your circuit for at least k=4 and k=5.
4. PDF files containing timing waveforms from the functional simulation demonstrating the correct operation of your circuit for k=4 and k=5.
5. FPGA resource utilization (as defined in Tasks 6 and D above), for k=4, 5, and 16.