Midterm Exam ECE 448
Spring 2021
Wednesday, March 10
15 points

Instructions:
Zip all your deliverables into an archive <last_name>.zip and submit it through Blackboard no later than Wednesday, March 10, 10:10 PM EST.

Textual Description

A circuit capable of sorting a set of 8 N-bit numbers is specified below using its

- Interface
- Table of input/output ports
- Block diagram of the Datapath
- Pseudocode
- Interface with the division into the Datapath and Controller
- ASM chart of the Controller.

Interface:

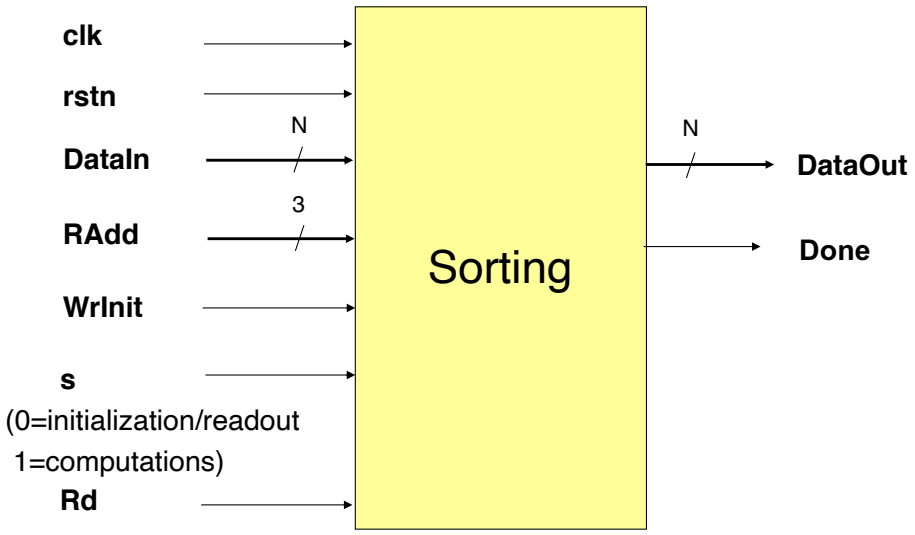
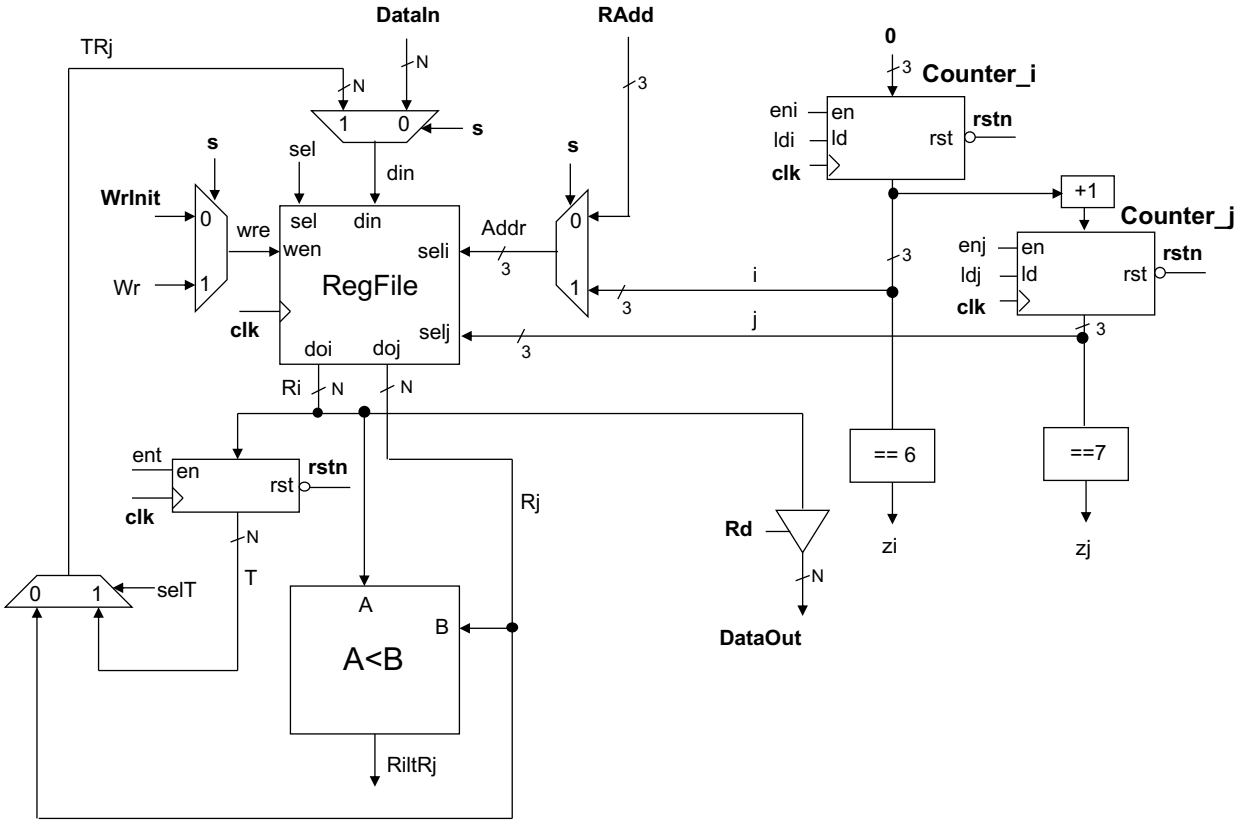


Table of input/output ports:

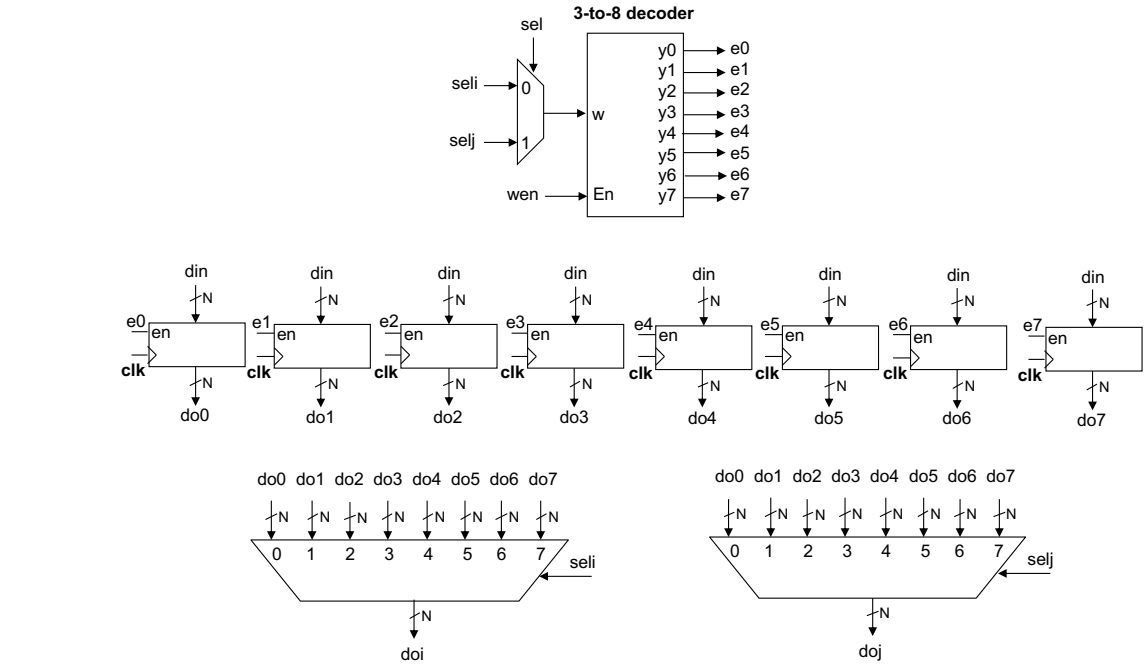
Port	Width	Meaning
clk	1	System clock
rstn	1	System reset – clears internal registers. Active low.
DataIn	N	Input data bus
RAdd	3	Address of the internal memory where input data is stored
WrInit	1	Synchronous write control signal
s	1	Operating mode: 0 = initialization, 1 = computations.
Rd	1	Read enable. 0 = high impedance on the output bus, 1 = valid output on the output data bus.
DataOut	N	Output data bus used to read results
Done	1	Asserted when all results are ready

Block diagram of the Datapath:

Main Circuit:



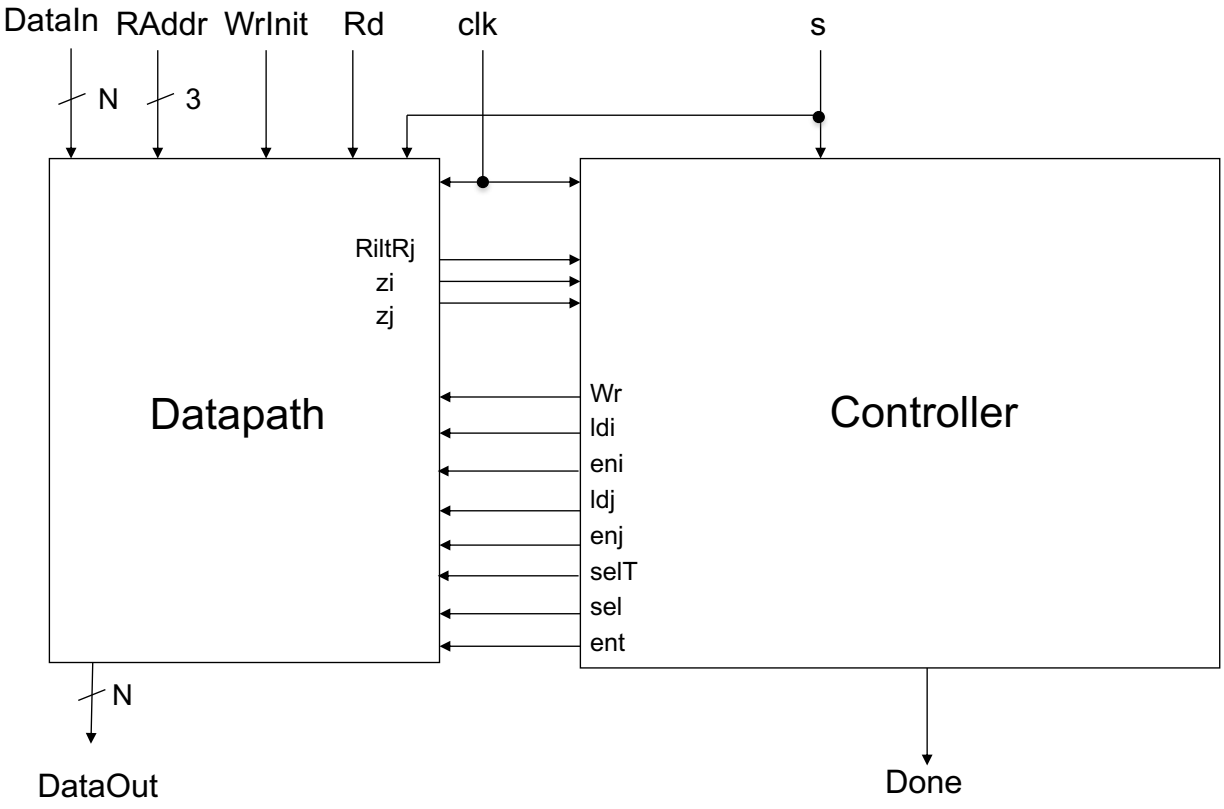
RegFile:



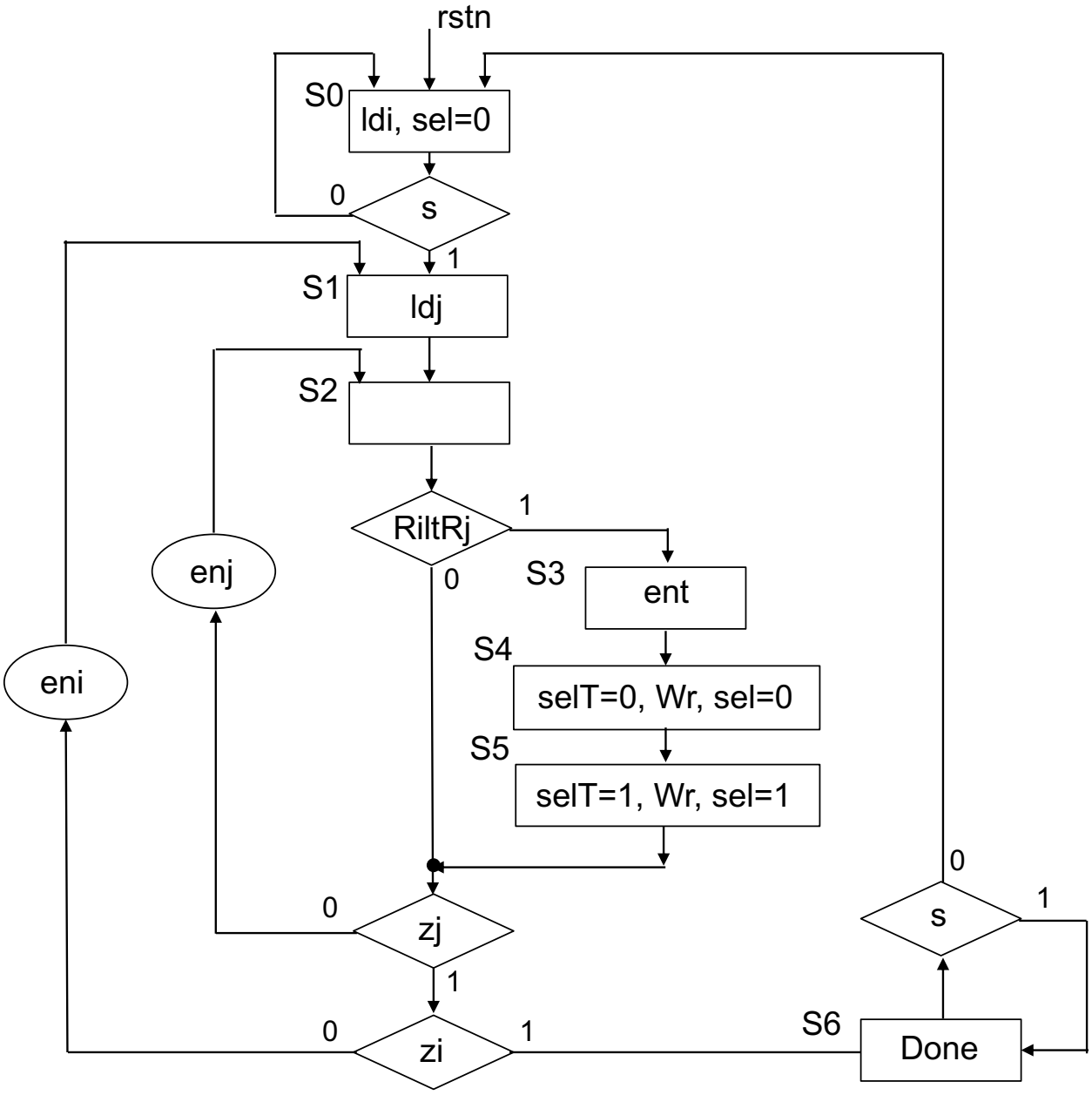
Pseudocode:

```
wait for s=1
for i=0 to 6 do
    for j=i+1 to 7 do
        if Ri < Rj then
            T = Ri
            Ri = Rj
            Rj = T
        end if
    end for
end for
Done
wait for s=0
go to the beginning
```

Interface with the division into the Datapath and Controller:



ASM chart of the controller:



Required Tasks:

Perform the following tasks:

1. Write a synthesizable VHDL code representing the specified above circuit.
2. Write a testbench verifying the operation of your circuit for at least two sets of eight 16-bit integers.
3. Perform functional simulation of your circuit and use it to debug your VHDL code. Take a printout of the waveforms showing the entire operation.
4. Synthesize your circuit.
5. Implement your circuit using
    a. FPGA family: Artix-7
    b. Part name: XC7A35TCPG236-1
    c. Speed Grade: -1
6. Based on the implementation reports, determine the number of CLB slices, LUTs, flip-flops, and pins used by the circuit.
7. Determine the resource utilization of your circuit for N=16 and N=32.

Deliverables:

1. VHDL code of your entire circuit.
2. VHDL code of your testbench, capable of verifying the operation of your circuit for at least N=16.
3. PDF files containing timing waveforms from the functional simulation demonstrating the correct operation of your circuit for N=16.
4. FPGA resource utilization (as defined in Tasks 6 and D above), for N=16 and N=32.