Midterm Exam ECE 448
Spring 2023
Friday, March 3
15 points

Instructions:
Zip all your deliverables into an archive <last_name>.zip and submit it through Blackboard no later than Friday, March 3, 11:20 AM EST.

Textual Description

Design, implement, and verify a **16-bit Binary Counter** unit, based on the following specification:

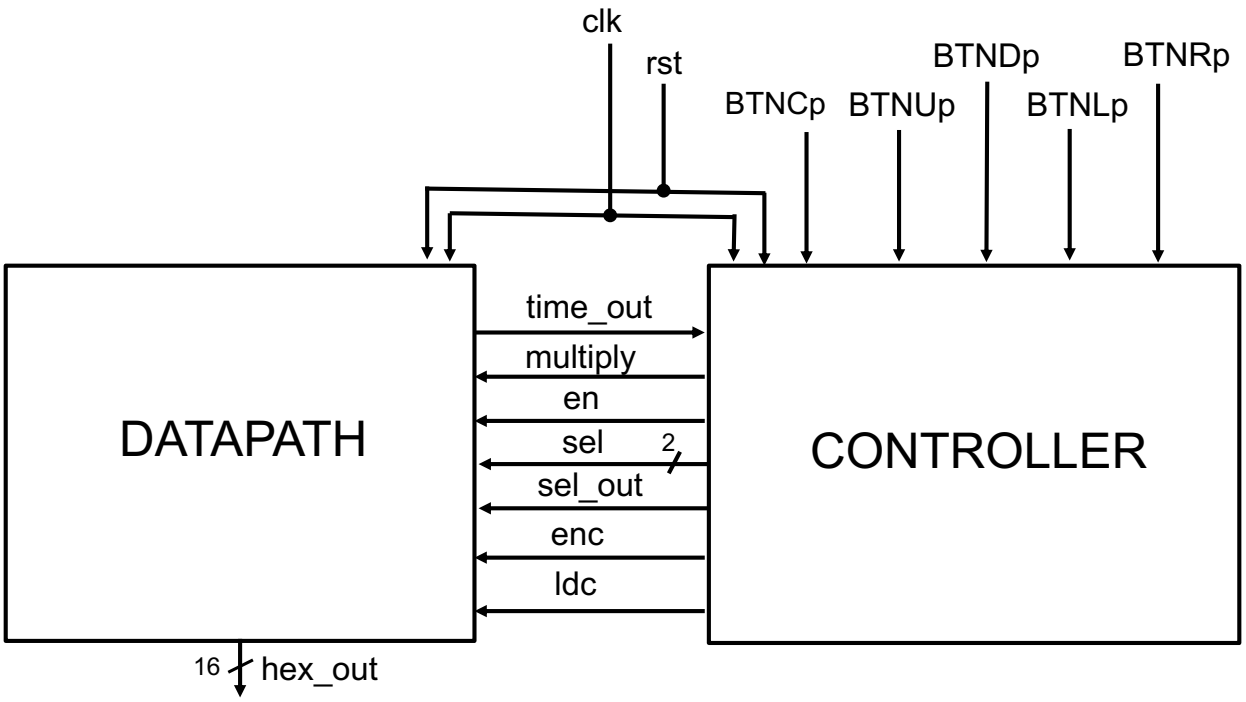
- BTNCp – toggling between addition and multiplication
- BTNUp – adding 2 or multiplying by 2
- BTNDp – adding 3 or multiplying by 3
- BTNLp – adding 5 or multiplying by 5
- BTNRp – adding 7 or multiplying by 7

The current value of the counter should be provided in hexadecimal notation at the output hex_out. After reset, the counter should be set to "0000" and the mode to addition.

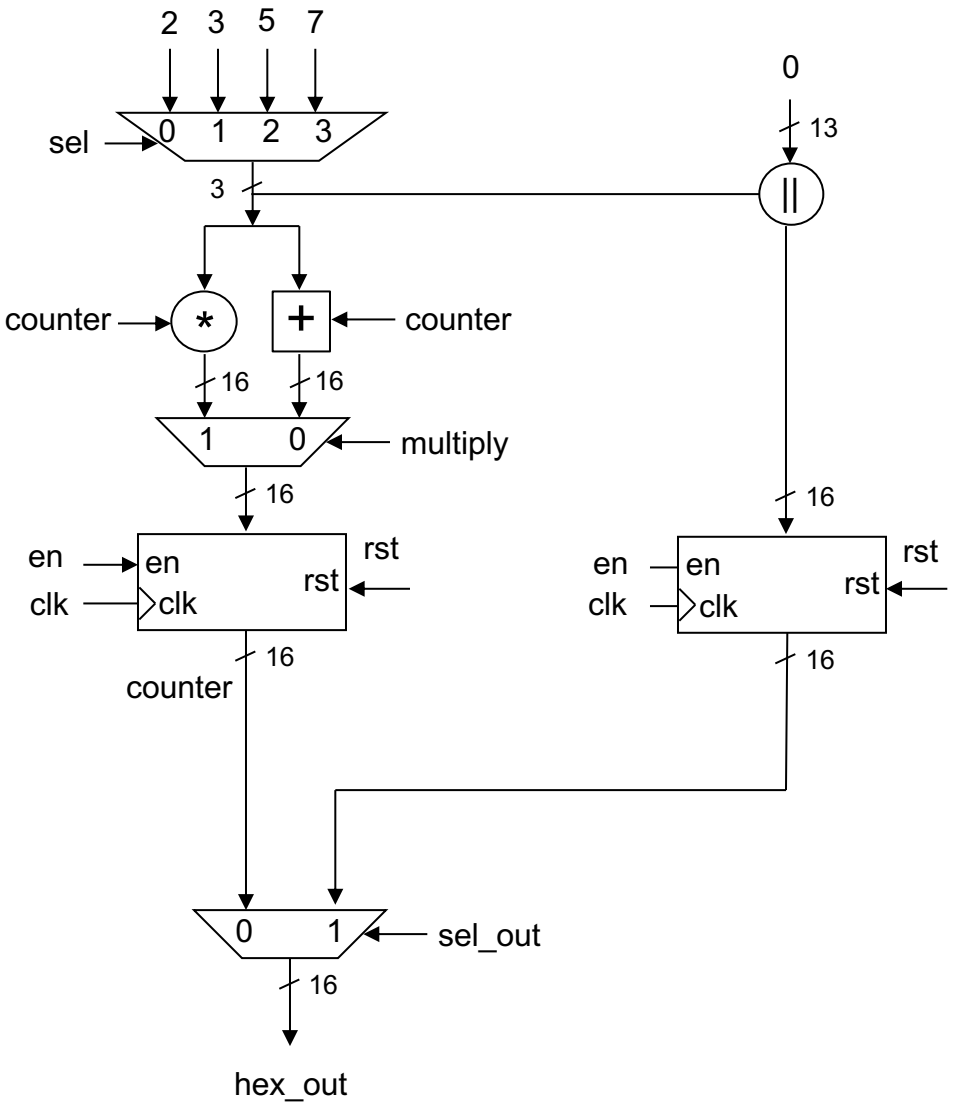
After any of the inputs representing an addition/multiplication amount (i.e., BTNUp, BTNDp, BTNLp, or BTNRp) is active for one clock period, the corresponding amount, represented in hexadecimal notation using 16 bits (i.e., 0002, 0003, 0005, 0007), should be displayed for 10 clock cycles, and then, the output hex_out should be equal to an updated value of the counter.

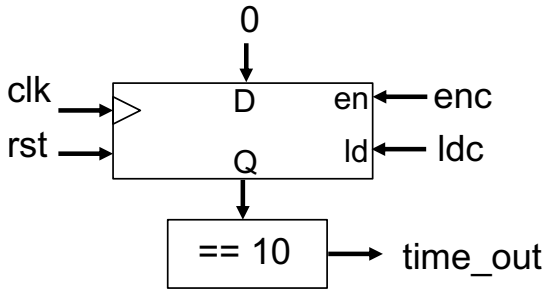
Please note that all additions and multiplications are performed modulo 2^{16}, which simply means that all bits of the results with indices 16 and higher are discarded and only 16 least significant bits are passed to the outputs of the adder and multiplier, respectively.

Interface with the division into the Datapath and Controller:

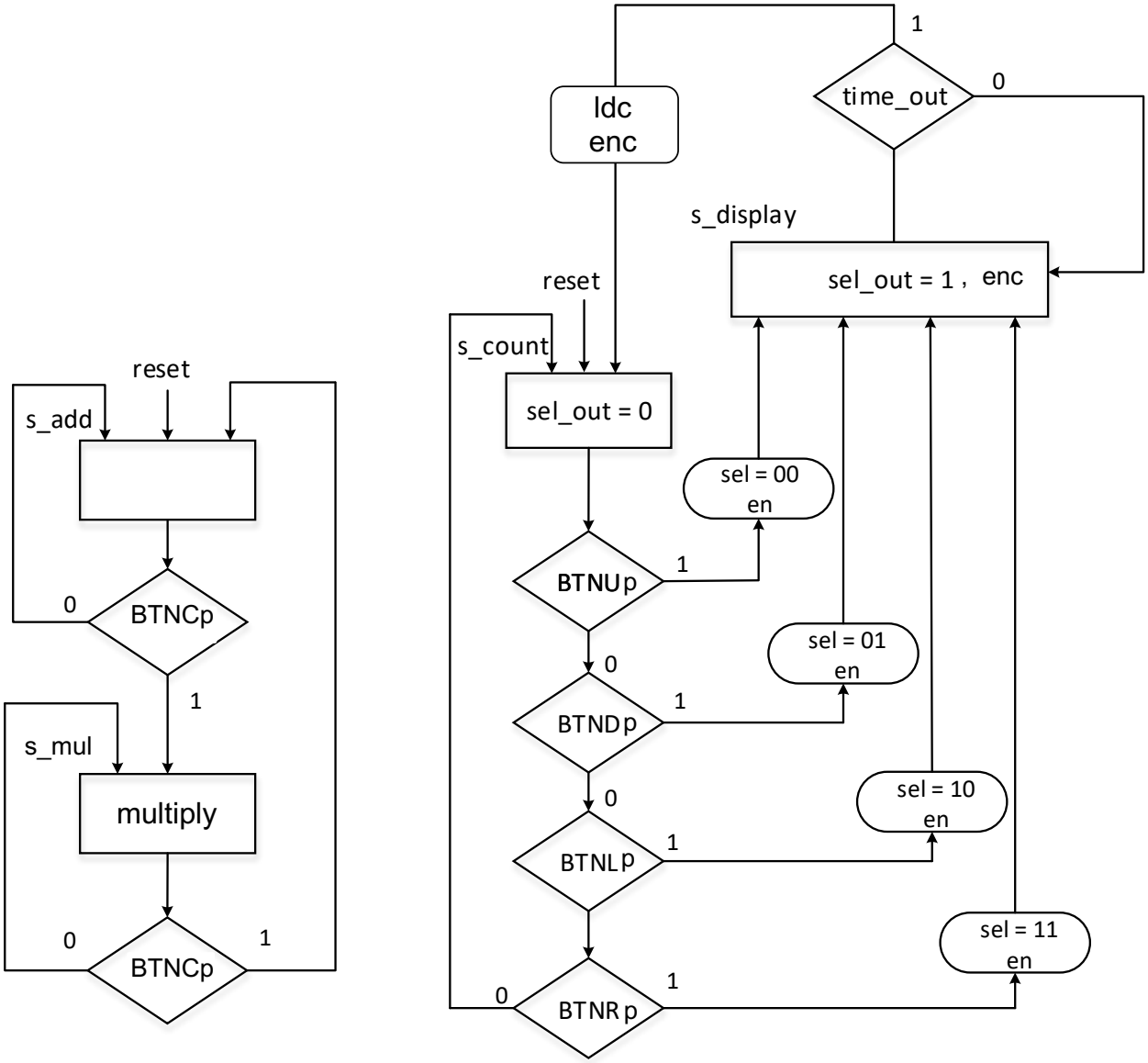


Block diagram of the Datapath





ASM chart of the controller:



Required Tasks:

Perform the following tasks:

1. Write synthesizable VHDL code representing the specified above circuit.
2. Write a testbench verifying the operation of your circuit.
3. Perform a behavioral simulation of your circuit and use it to debug your VHDL code. Take a printout of waveforms demonstrating the correct operation of the circuit.
4. Set the target clock frequency to 100 MHz using a simple XDC file.
5. Synthesize and implement your circuit using
    a. FPGA family: Artix-7
    b. Part name: XC7A35TCPG236-1
    c. Speed Grade: -1
6. Based on the implementation reports, determine
    a. the number of LUTs, flip-flops, and pins used by the circuit
    b. worst negative slack.
7. Verify the operation of your circuit using the post-implementation timing simulation. Take printout of waveforms demonstrating the correct operation of the circuit.

Deliverables:

1. Synthesizable VHDL code.
2. Testbench.
3. XDC file.
4. Resource utilization and the Worst Negative Slack reported by Vivado.
5. Timing waveforms obtained from the behavioral and timing simulations, demonstrating the correct operation of the circuit (stored as PDF files).