Midterm Exam ECE 448
Spring 2023
Monday, March 6
15 points

Instructions:
Zip all your deliverables into an archive <last_name>.zip and submit it through Blackboard no later than Monday, March 6, 11:40 AM EST.

Textual Description

Design, implement, and verify the Midterm_Exam unit defined as follows:

After the asynchronous reset, `rst,` becomes active, the 8-bit register `accum` is set to zero.

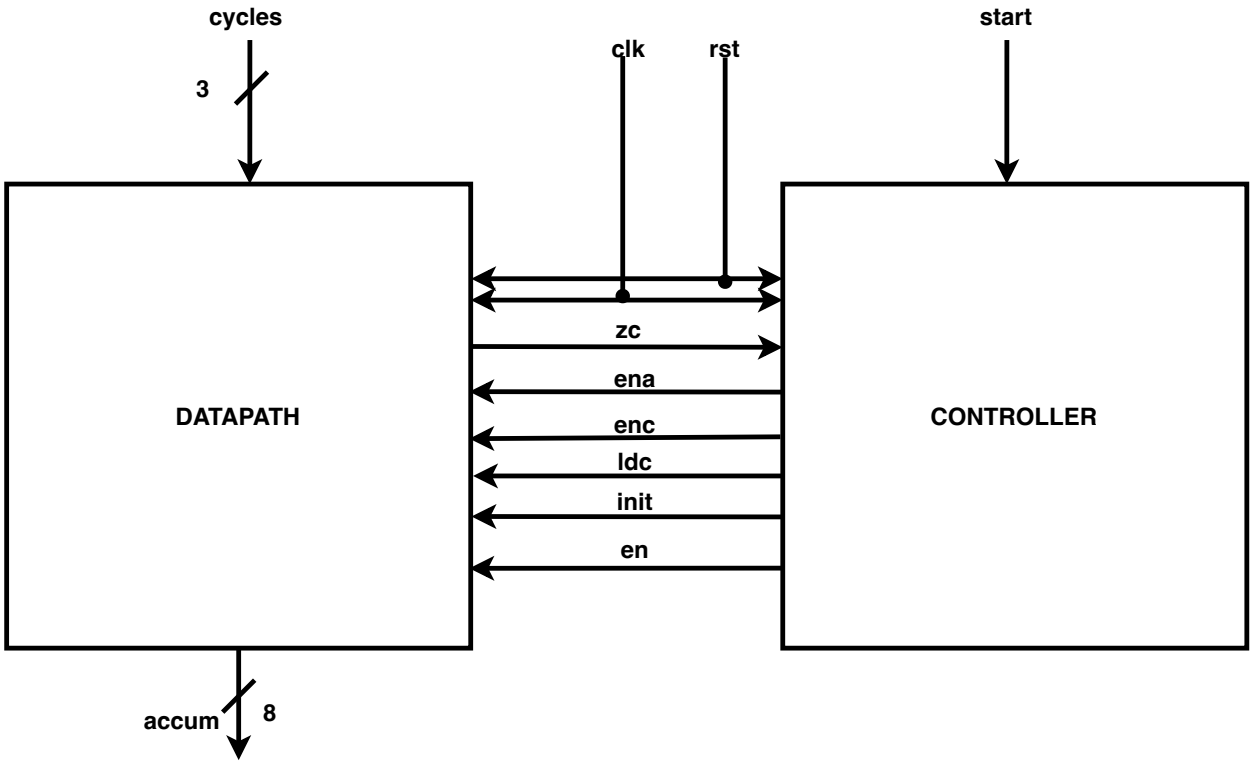
Afterward, when `start=1`, the LFSR, shown in Fig. 1, is initialized by setting the synchronous input INIT to 1 for one clock cycle. At the same time, the value of the input `cycles` becomes an initial value of the 3-bit down counter, `cnt` (shown in Fig. 2). Then, `cnt` is enabled and counts down. When `cnt` reaches zero, the following operation is performed

`accum` = (`accum` + `LFSR(7..0)`) mod 2^8 when `LFSR(8)` = '0'
`accum` = (`accum` * `LFSR(7..0)`) mod 2^8 when `LFSR(8)` = '1'.

Hint: The operation `X` mod 2^8 returns 8 least significant bits of `X` and discards all remaining bits of `X`.

Afterward, the circuit waits for another active value of `start` and another 3-bit value of the input `cycles`. The operation of the circuit continues indefinitely.

Interface with the division into the Datapath and Controller:



Block diagram of the Datapath

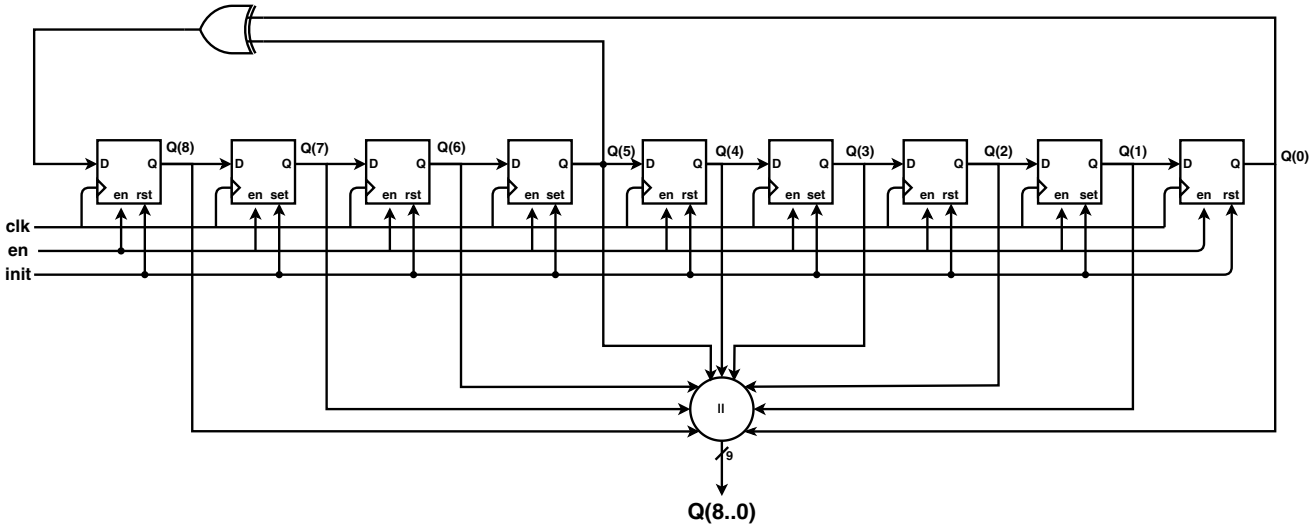


Fig. 1: 9-bit LFSR

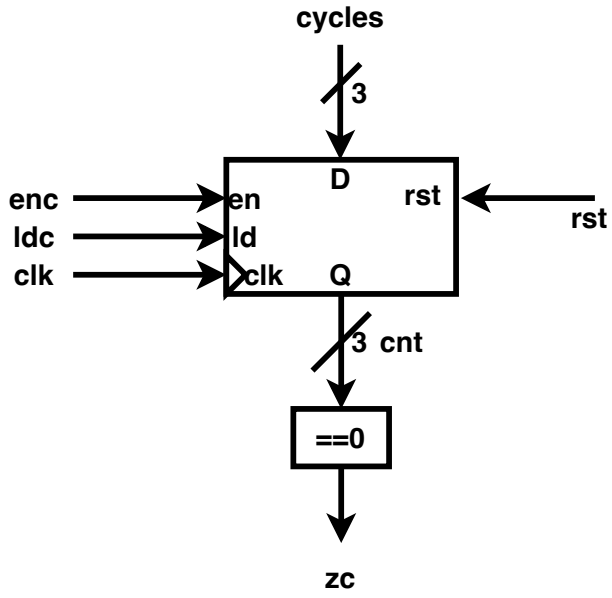


Fig. 2: 3-bit Down Counter

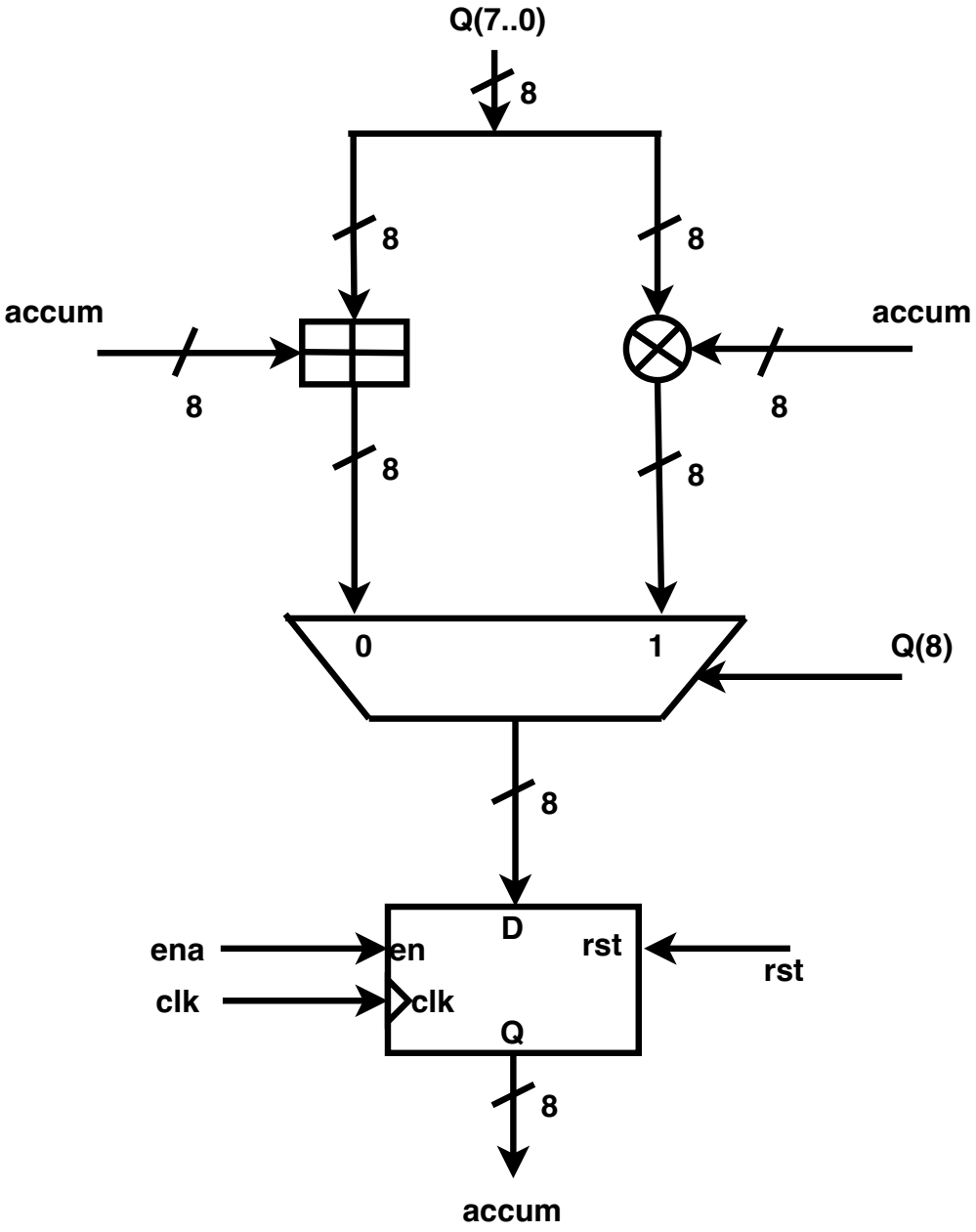
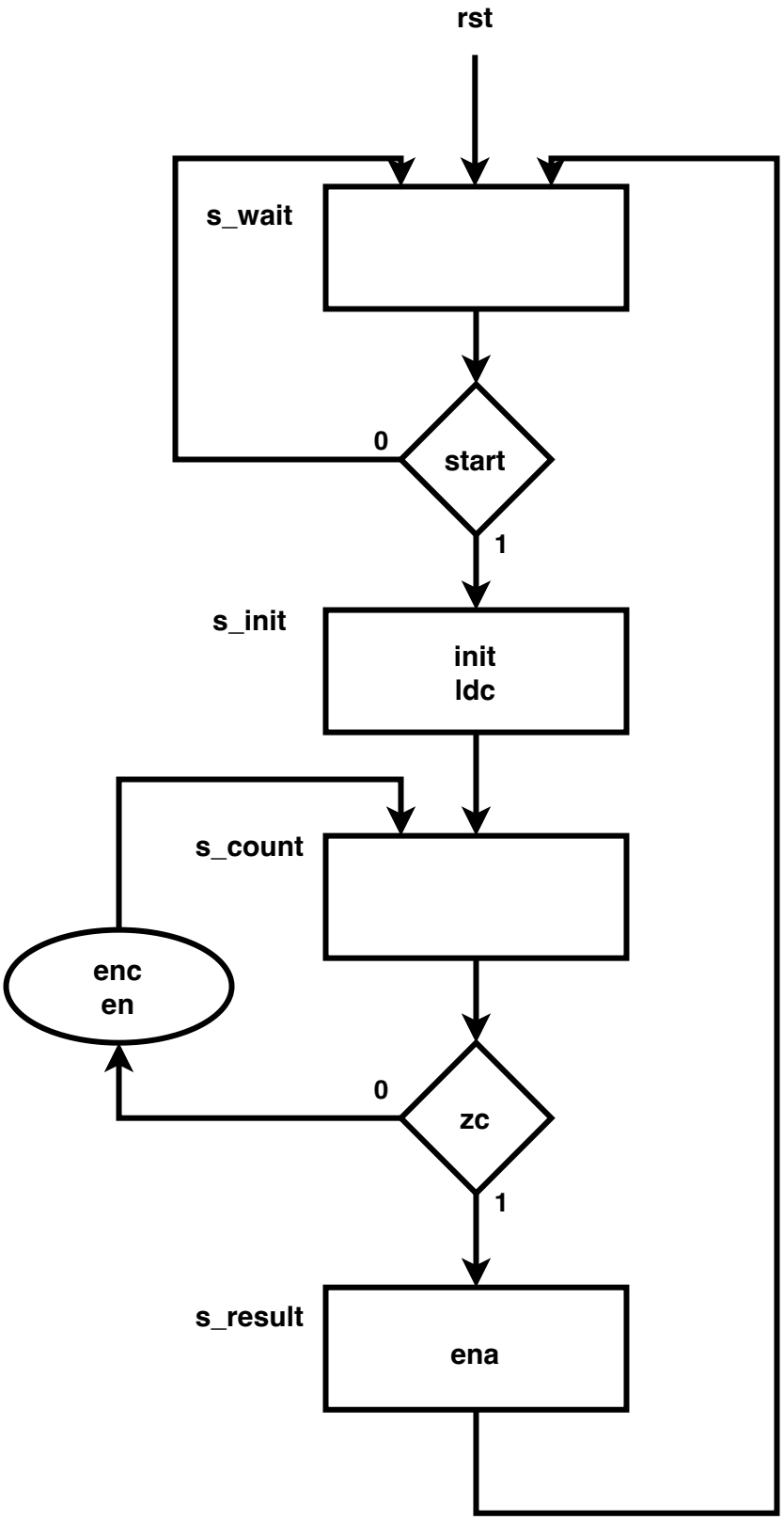


Fig. 3: Adder/Multiplier and Accumulator

ASM chart of the controller:



Required Tasks:

Perform the following tasks:

1. Write synthesizable VHDL code representing the specified above circuit.
2. Write a testbench verifying the operation of your circuit.
3. Perform a behavioral simulation of your circuit and use it to debug your VHDL code. Take a printout of waveforms demonstrating the correct operation of the circuit.
4. Set the target clock frequency to 100 MHz using a simple XDC file.
5. Synthesize and implement your circuit using
    a. FPGA family: Artix-7
    b. Part name: XC7A35TCPG236-1
    c. Speed Grade: -1
6. Based on the implementation reports, determine
    a. the number of LUTs, flip-flops, and pins used by the circuit
    b. worst negative slack.
7. Verify the operation of your circuit using the post-implementation timing simulation. Take printout of waveforms demonstrating the correct operation of the circuit.

Deliverables:

1. Synthesizable VHDL code.
2. Testbench.
3. XDC file.
4. Resource utilization and the Worst Negative Slack reported by Vivado.
5. Timing waveforms obtained from the behavioral and timing simulations, demonstrating the correct operation of the circuit (stored as PDF files).