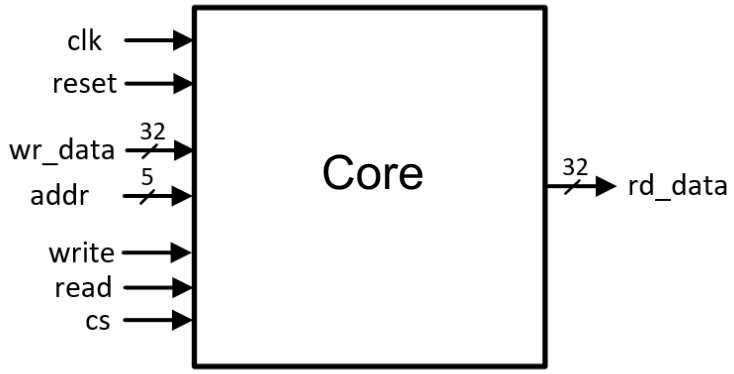
ECE 448
Spring 2023

Homework 1
due Sunday, May 14, 2023, 11:59 PM

Draw a detailed internal block diagram of an FPro MMIO Core with the following interface and the Memory & I/O Register Map shown on the next page.

Interface:



Assumptions:

- **Registers must be implemented using actual registers, not memory.**
- **RegA is an 18-bit read-only register.**
- **RegB can be written to and read from. This register has the width of 32 bits.**
- **CounterA is an 18-bit counter. Writing to a counter initializes this counter. Reading from a counter reads its current value. Assume that initializing a counter requires only an active value of the load input.**
- **SrlA is an 18-bit shift register, shifting to the left, with parallel load, parallel output, serial input and serial output, and asynchronous reset active low. Assume that the parallel load requires only an active value of the load input. The processor should be able to initialize this shift register by writing to the respective address and read its parallel output by reading from the same address.**
- **GoX and GoY are 1-bit write-only flags located at the two least significant bit locations (1 and 0, respectively) at the address 5.**
- **Ready is a 1-bit read-only flag located at the most significant bit location (31) at the address 5.**

Use the simplified address decoding scheme.

Memory & I/O Register Map: