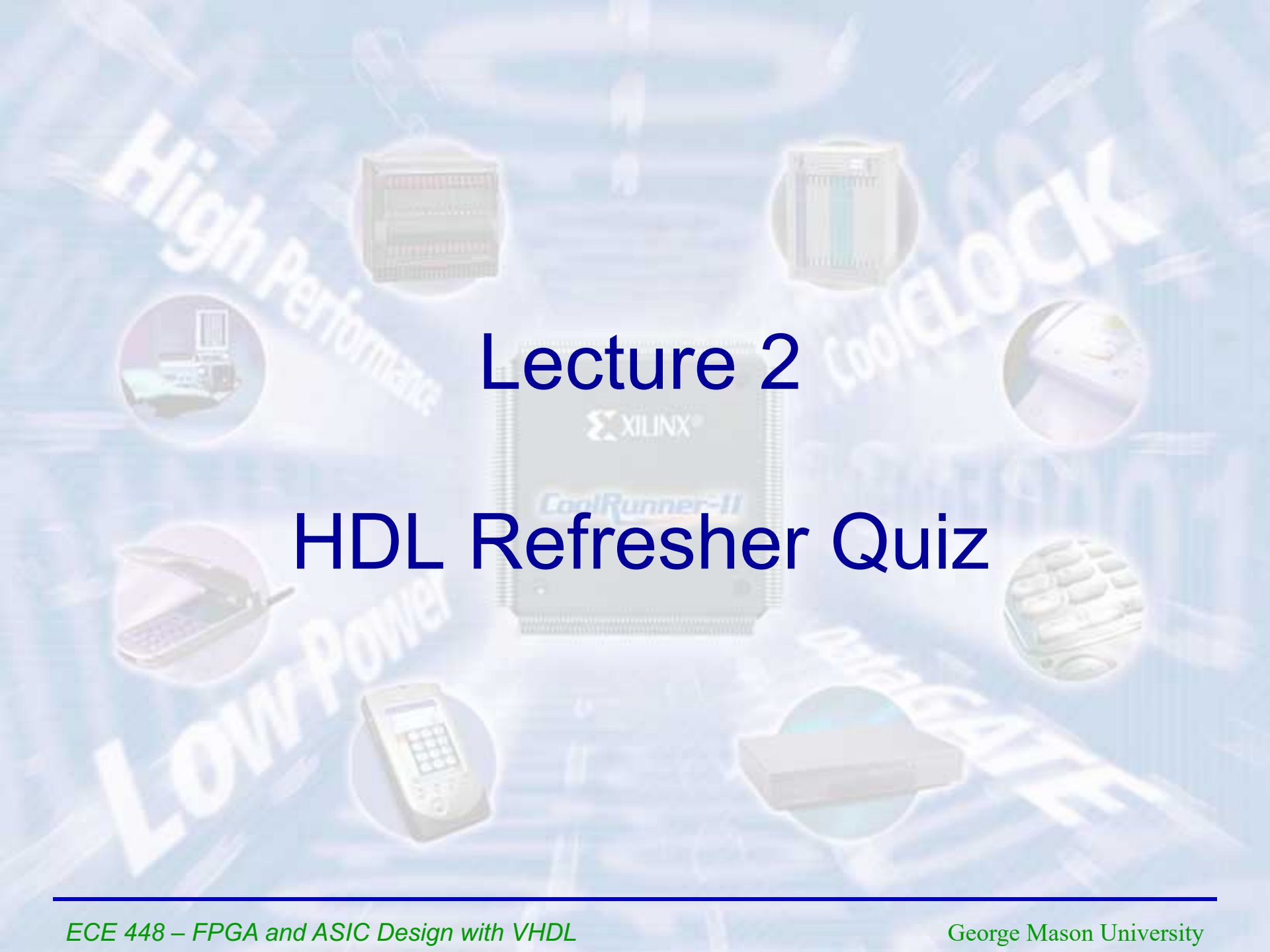


Lecture 2

HDL Refresher Quiz

Rules

- If you believe that you know a correct answer, please raise your hand
- I will select *one or more* students (independently whether an answer given by the first student is correct or incorrect)
- Please, identify yourself by **first** name and give an answer
- **Correct answer = 1 bonus point**

Question 1

- VHDL stands for

  .....

VHDL

- **VHDL** is an acronym for **V**HSIC (**V**ery **H**igh **S**peed **I**ntegrated **C**ircuit) **H**ardware **D**escription **L**anguage

Question 2

- VHDL was developed around
  - A. 1975
  - B. 1985
  - C. 1993
  - D. 2000
  - E. 2008

A Brief History of VHDL

- July 1983: a DoD contract for the development of VHDL awarded to
  - Intermetrics
  - IBM
  - Texas Instruments
- August 1985: VHDL Version 7.2 released
- December 1987:

  VHDL became IEEE Standard 1076-1987 and in 1988 an ANSI standard

Major versions of VHDL

- IEEE-1076 1987
- IEEE-1076 1993 ← most commonly supported by CAD tools
- IEEE-1076 2008 ← supported by the new generation of CAD tools, such as Xilinx Vivado

Question 3

- Syntax of VHDL is based on the programming language called

  .....

Question 4

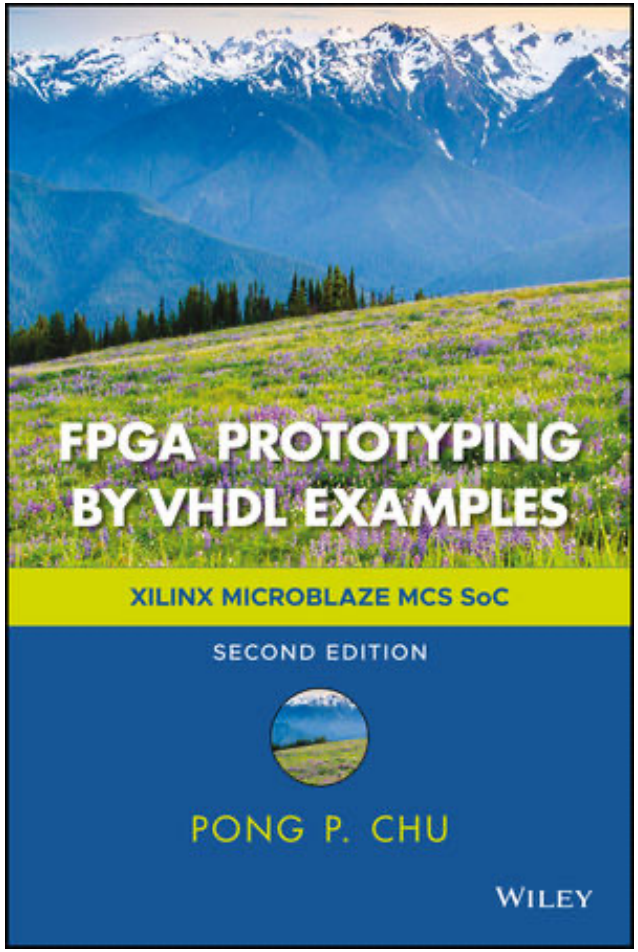
- Two currently most popular hardware description languages are:

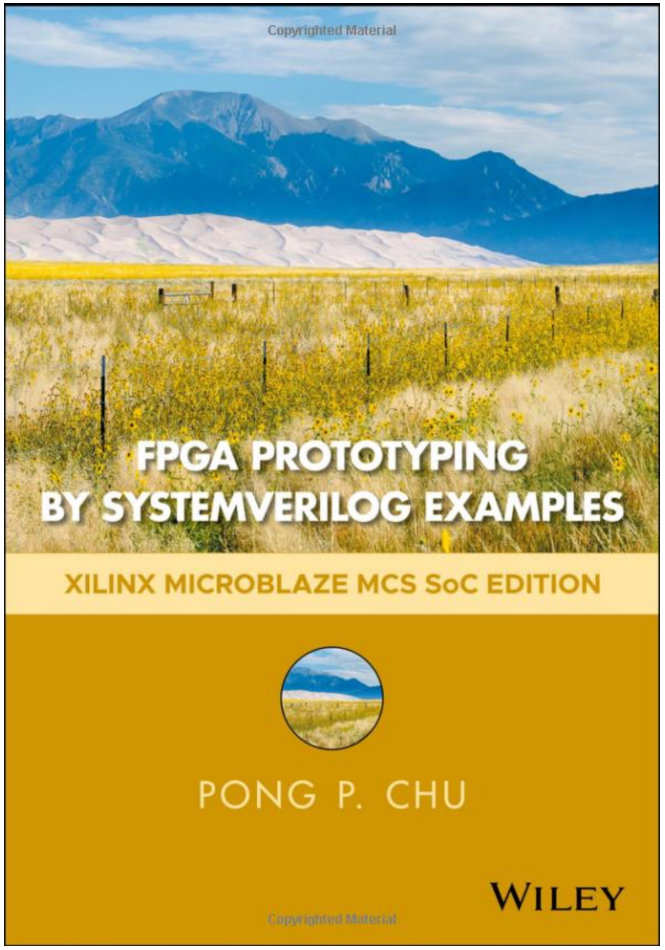
  VHDL and ……

VHDL vs. Verilog

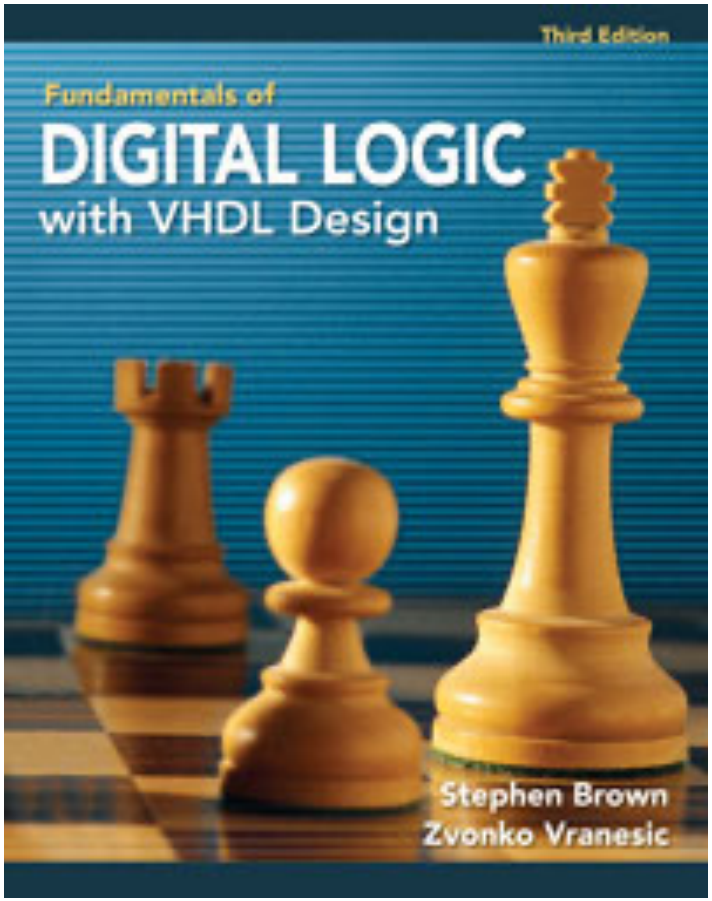
Government Developed	Commercially Developed
Ada based	C based
Strongly Typed	Loosely typed
Case-insensitive	Case-sensitive
More difficult to learn	Easier to Learn

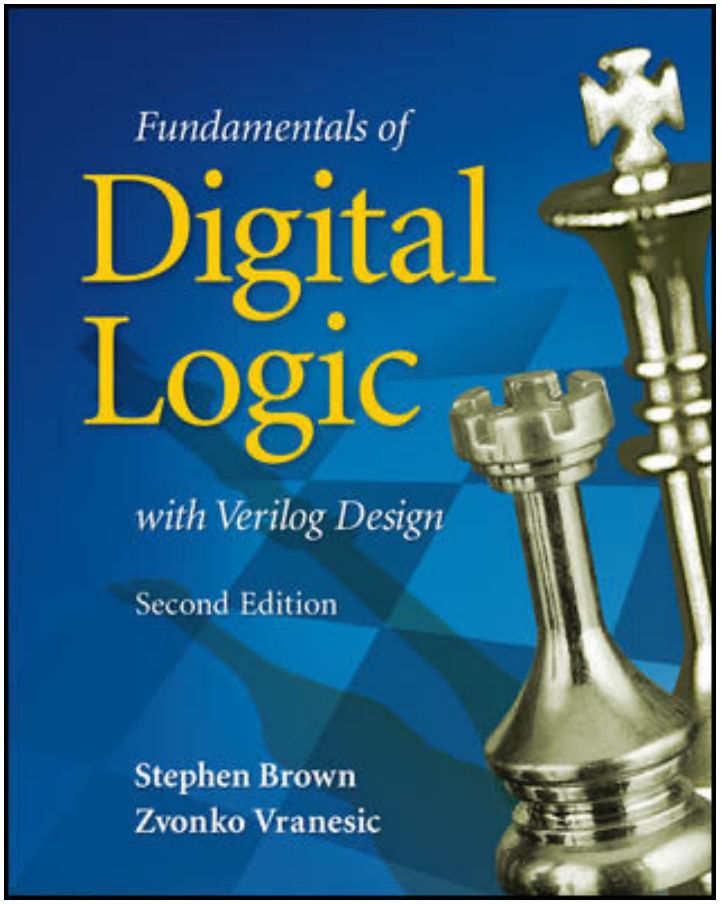
How to learn Verilog by yourself ?





How to learn Verilog by yourself ?





Question 5

- VHDL is
  - A. case sensitive
  - B. case insensitive

Question 6

Which of the following identifiers are invalid in VHDL?

A. `7segment_display`
B. `A87372477424`
C. `/reset`
D. `And_or_gate`
E. `AND__OR__NOT`
F. `My adder`

Naming and Labeling

General rules of thumb (according to VHDL-87)

1. All names should start with an alphabet character (a-z or A-Z)
2. Use only alphabet characters (a-z or A-Z) digits (0-9) and underscore (_)
3. Do not use any punctuation or reserved characters within a name (!, ?, ., &, +, -, etc.)
4. Do not use two or more consecutive underscore characters (__) within a name (e.g., Sel__A is invalid)
5. All names and labels in a given entity and architecture must be unique

Question 7

The notation for comments in VHDL is

A. /* */
B. --
C. //
D. **

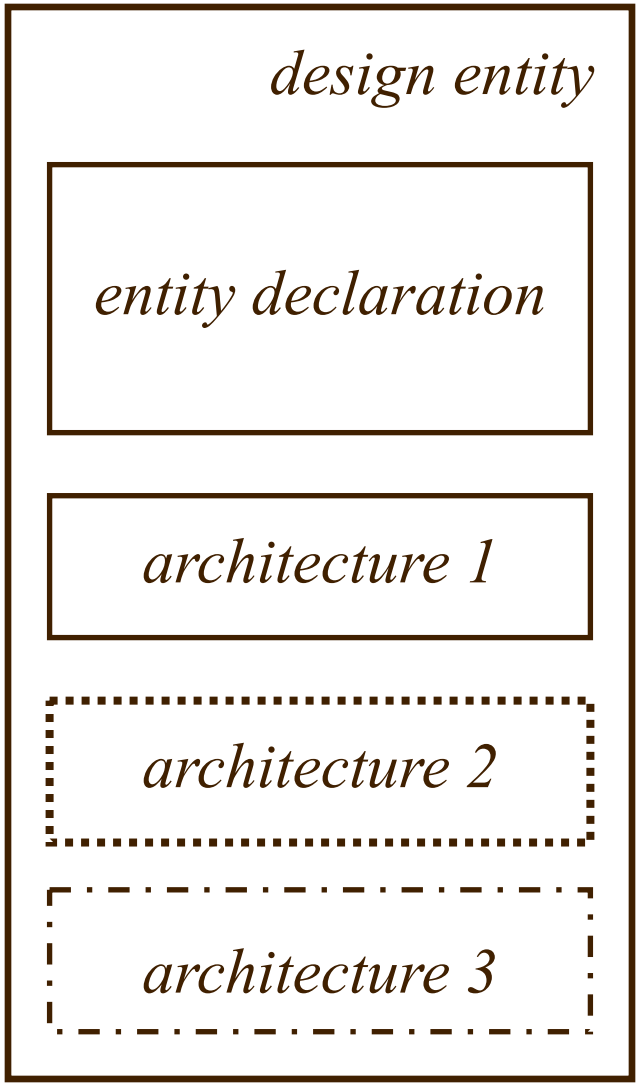
Question 8

True or false?

A. One architecture can have multiple entity declarations

B. One entity declaration can have multiple architectures

Design Entity



Design Entity - most basic building block of a design.

One *entity* can have many different *architectures.*

Question 9

What are valid port **modes** in VHDL**?**

Question 10

What are the recommended port **types** in synthesizable VHDL**?**

STD_LOGIC Rules

- In ECE 448, use **std_logic** or **std_logic_vector** for all entity input or output ports
  - Do not use integer, unsigned, signed, bit for ports
  - You can use them inside of architectures if desired
  - You can use them in generics
- Instead use std_logic_vector and a conversion function inside of your architecture

  [Consistent with OpenCores Coding Guidelines]

Question 11

What are 3 most commonly used **libraries?**

Libraries

- ieee

  Specifies multi-level logic system, including STD_LOGIC, and STD_LOGIC_VECTOR data types

Need to be explicitly declared

- std

  Specifies pre-defined data types (BIT, BOOLEAN, INTEGER, REAL, SIGNED, UNSIGNED, etc.), arithmetic operations, basic type conversion functions, basic text i/o functions, etc.

- work

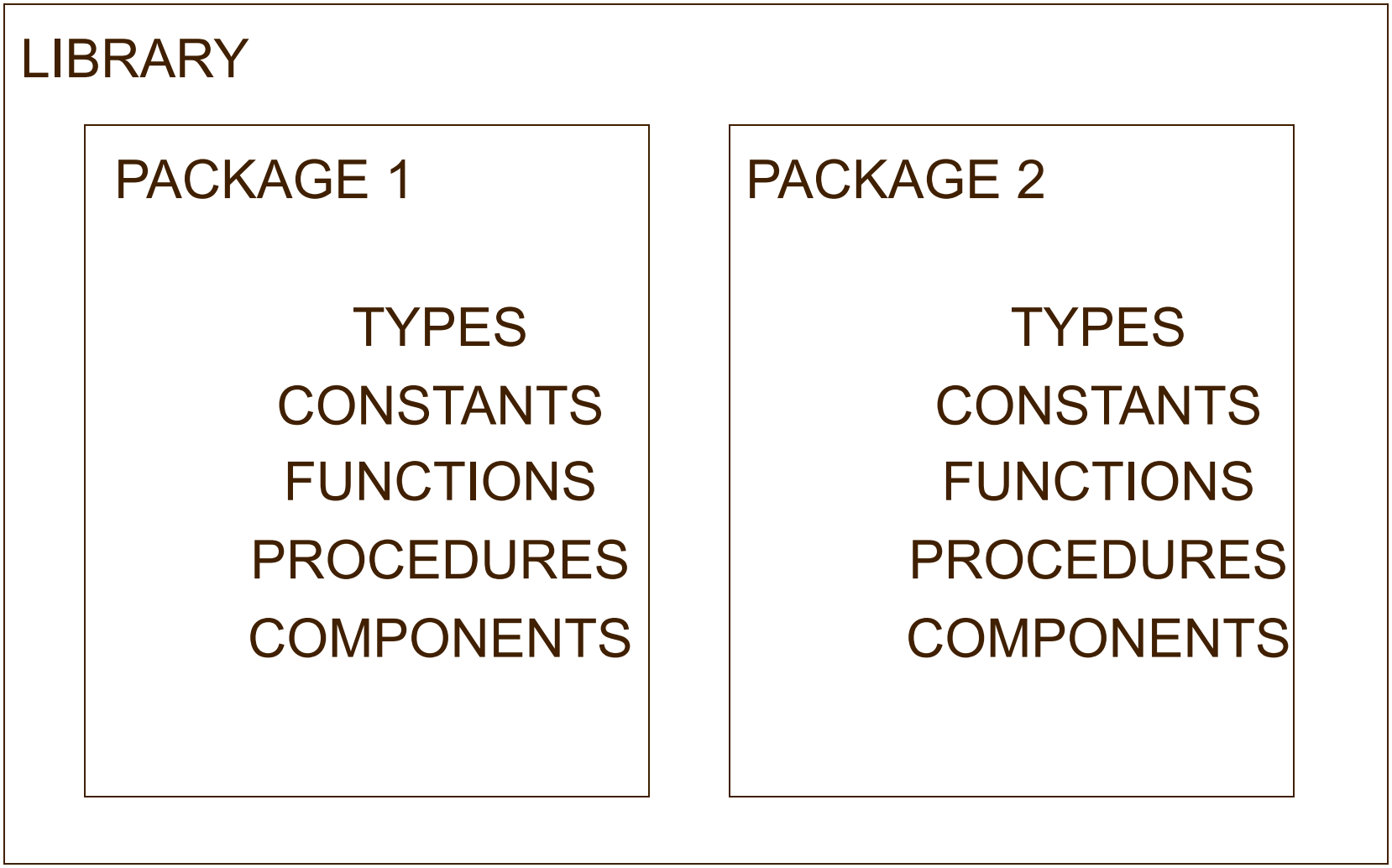
  Holds current designs after compilation

Visible by default

Question 12

What information is typically stored in packages?

Fundamental parts of a library



Question 13

Give a name of at least one commonly used **package**?

Library Declarations

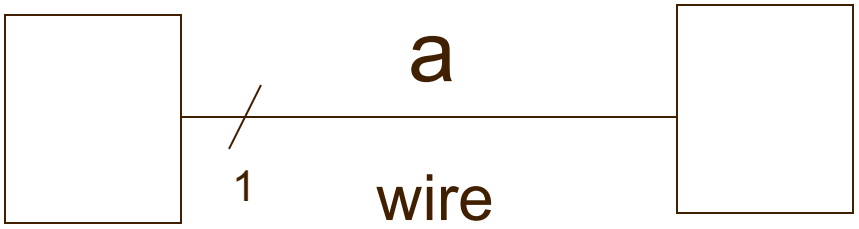
```
LIBRARY ieee;
USE ieee.std_logic_1164.all;

ENTITY nand_gate IS
     PORT(
          a    : IN STD_LOGIC;
          b    : IN STD_LOGIC;
          z    : OUT STD_LOGIC);
END nand_gate;

ARCHITECTURE dataflow OF nand_gate IS
BEGIN
     z <= a NAND b;
END dataflow;
```

Library declaration

Use all definitions from the package std_logic_1164

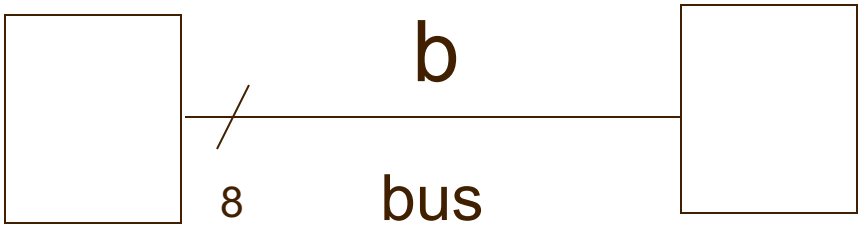
Question 14

What is an VHDL object that represents a **wire** connecting two components in a digital circuit?



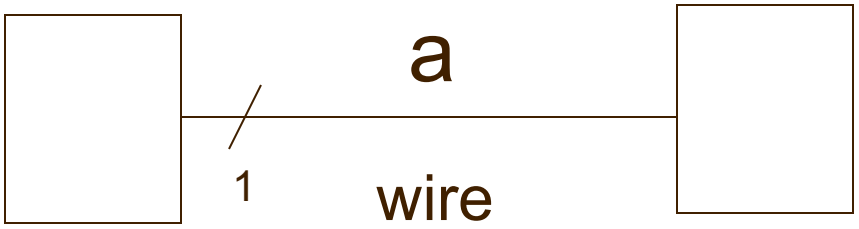
Question 15

What is an VHDL object that represents a **bus** connecting two components in a digital circuit?

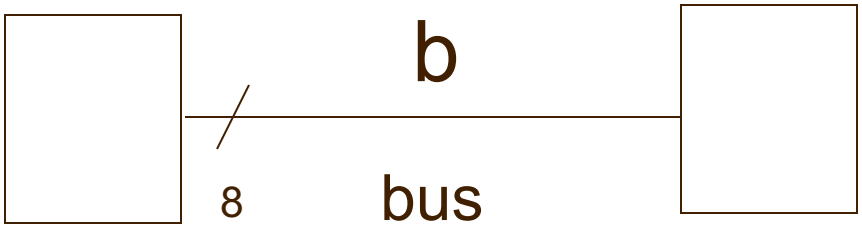


Signals

SIGNAL a : STD_LOGIC;



SIGNAL b : STD_LOGIC_VECTOR(7 DOWNTO 0);



Question 16

What is a notation for a hexadecimal number in VHDL?

A. 0xAB
B. ABH
C. 0AB
D. X"AB"
E. H"AB"

Question 17

What is a meaning of “&” in VHDL?

A. Bitwise AND
B. Logical AND
C. Bitwise OR
D. Logical OR
E. Concatenate

Question 18

Which type of VHDL description is based on the use of **concurrent statements**?

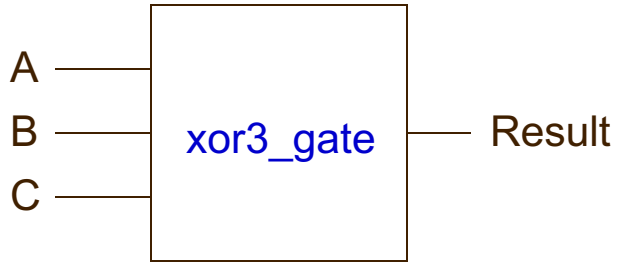
A. dataflow
B. structural
C. behavioral

Question 19

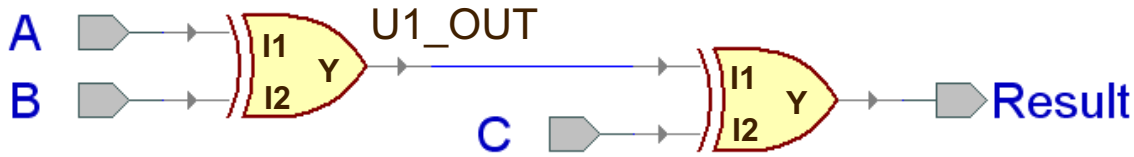
Which type of VHDL description is based on the use of **processes**?

A. dataflow
B. structural
C. behavioral

Question 20: Fill in the blanks

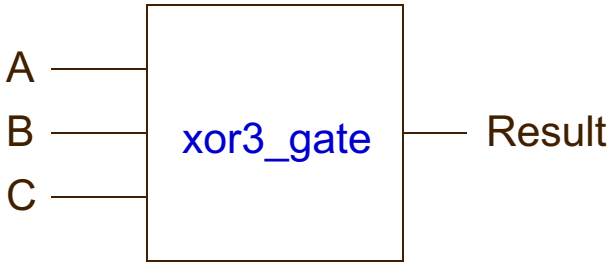


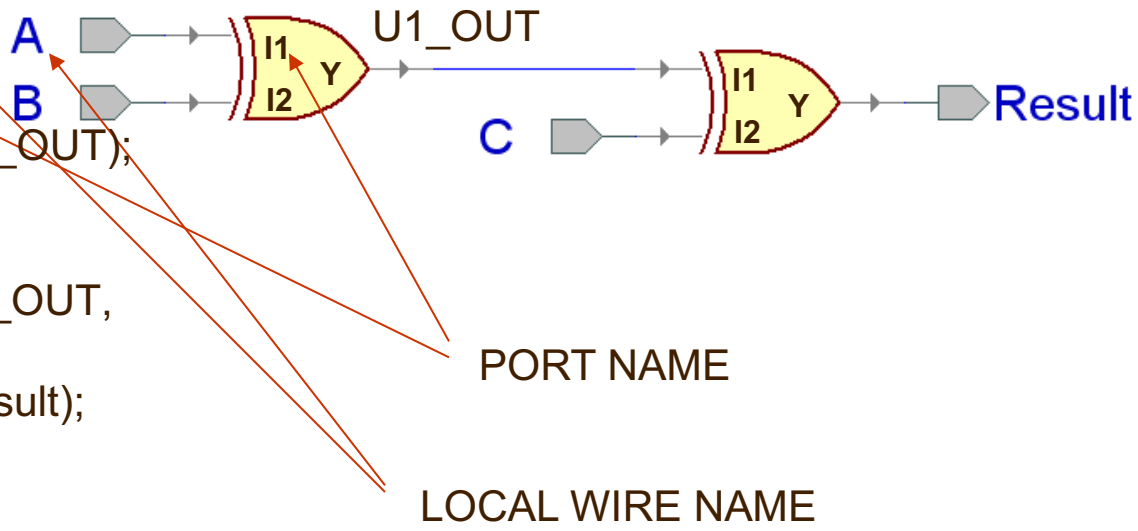

```
ARCHITECTURE structural OF xor3_gate IS
SIGNAL U1_OUT: STD_LOGIC;

BEGIN
    U1: entity work.xor2(dataflow)
            PORT MAP (…. => …..,
                      …. => …..,
                      ….  => ……);

    U2:  entity work.xor2(dataflow)
            PORT MAP (….. => …..,
                      ….. => ……,
                      …..  => ……);
END structural;
```



Structural Architecture in VHDL 93

```
ARCHITECTURE structural OF xor3_gate IS
SIGNAL U1_OUT: STD_LOGIC;

BEGIN
    U1: entity work.xor2(dataflow)
            PORT MAP (I1 => A,
                      I2 => B,
                      Y  => U1_OUT);

    U2:  entity work.xor2(dataflow)
            PORT MAP (I1 => U1_OUT,
                      I2 => C,
                      Y  => Result);
END structural;
```





Question 21

Which style of VHDL description is used in the following example?

```
ARCHITECTURE unknown OF xor3 IS
BEGIN
xor3: PROCESS (A, B, C)
BEGIN
    IF ((A XOR B XOR C) = '1') THEN
            Result <= '1';
    ELSE
            Result <= '0';
    END IF;
END PROCESS xor3;
END unknown;
```

Types of VHDL Description: Convention used in this class