Lecture 7a

Sequential Logic Refresher Quiz

Rules

- If you believe that you know a correct answer, please raise your hand
- I will select *one or more* students (independently whether an answer given by the first student is correct or incorrect)
- Please, identify yourself by **first** name and give an answer
- **Correct answer = 1 bonus point**

Question 1

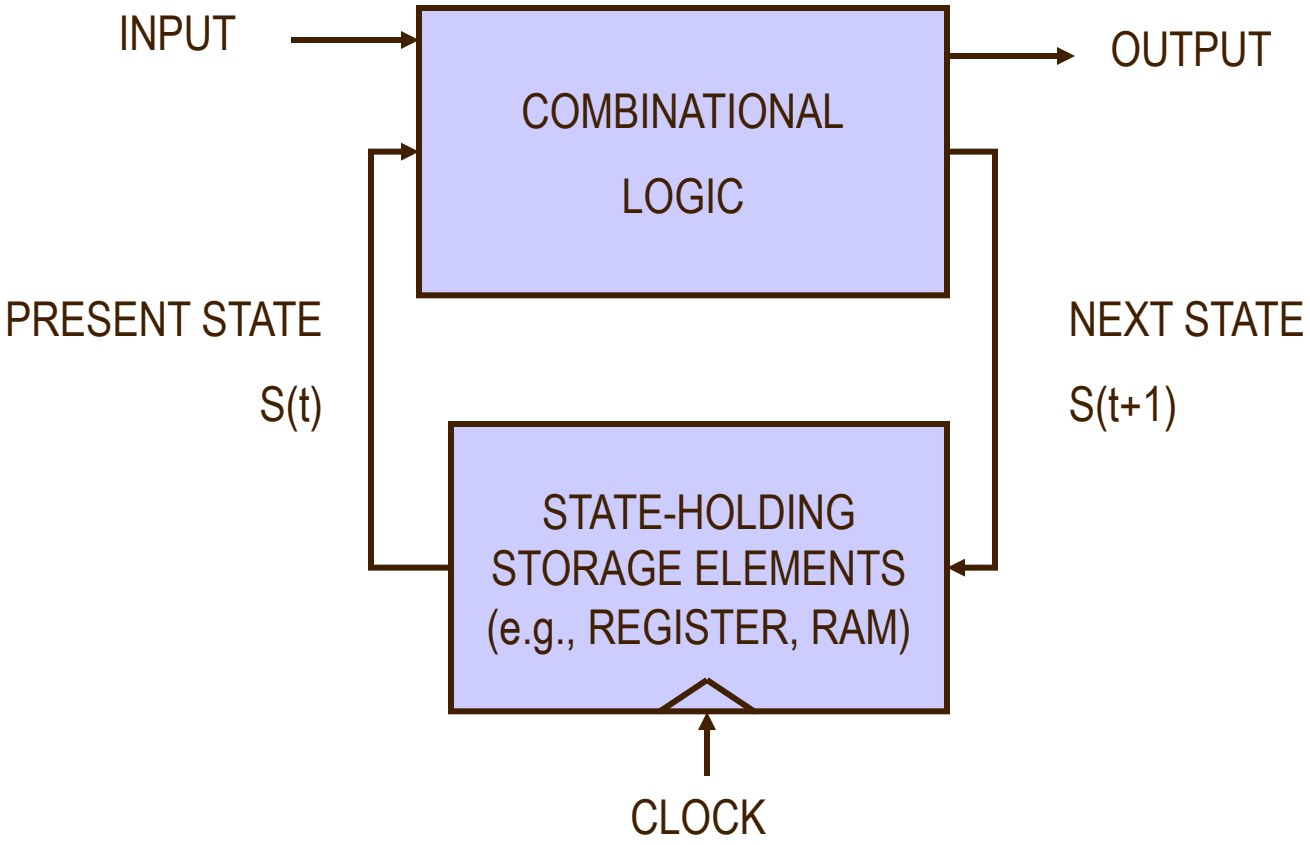
What is a difference between combinational logic and sequential logic?

Introduction to Sequential Logic

- Output depends on the current input and the internal state
- Past inputs effects the internal state
- Sequential circuits consist typically of
  - Storage elements (flip-flop, latch, register, RAM, etc.)
  - Combinational logic

Introduction (cont'd)

Main components of a typical synchronous sequential circuit (synchronous = uses a clock to keep circuits in lock step)



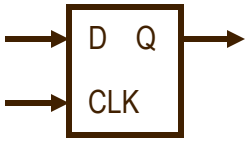
Question 2

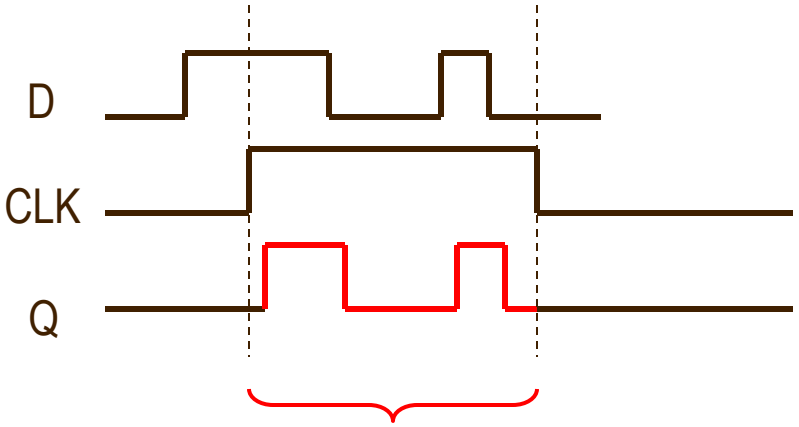
What is a difference between Latches and Flip-flops?

State-Holding Memory Elements

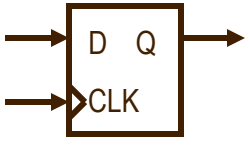
- Latch versus Flip Flop
  - Latches are level-sensitive: whenever clock is high, latch is transparent
  - Flip-flops are edge-sensitive: data passes through (i.e., data is sampled) only on a rising (or falling) edge of the clock
  - Latches cheaper to implement than flip-flops
  - Flip-flops are easier to design with than latches
- In this course, primarily use D flip-flops

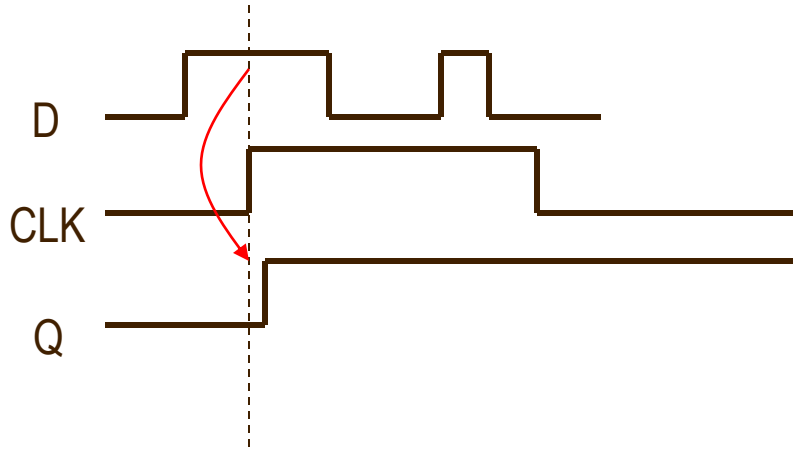
D Latch vs. D Flip-Flop





Latch transparent when clock is high



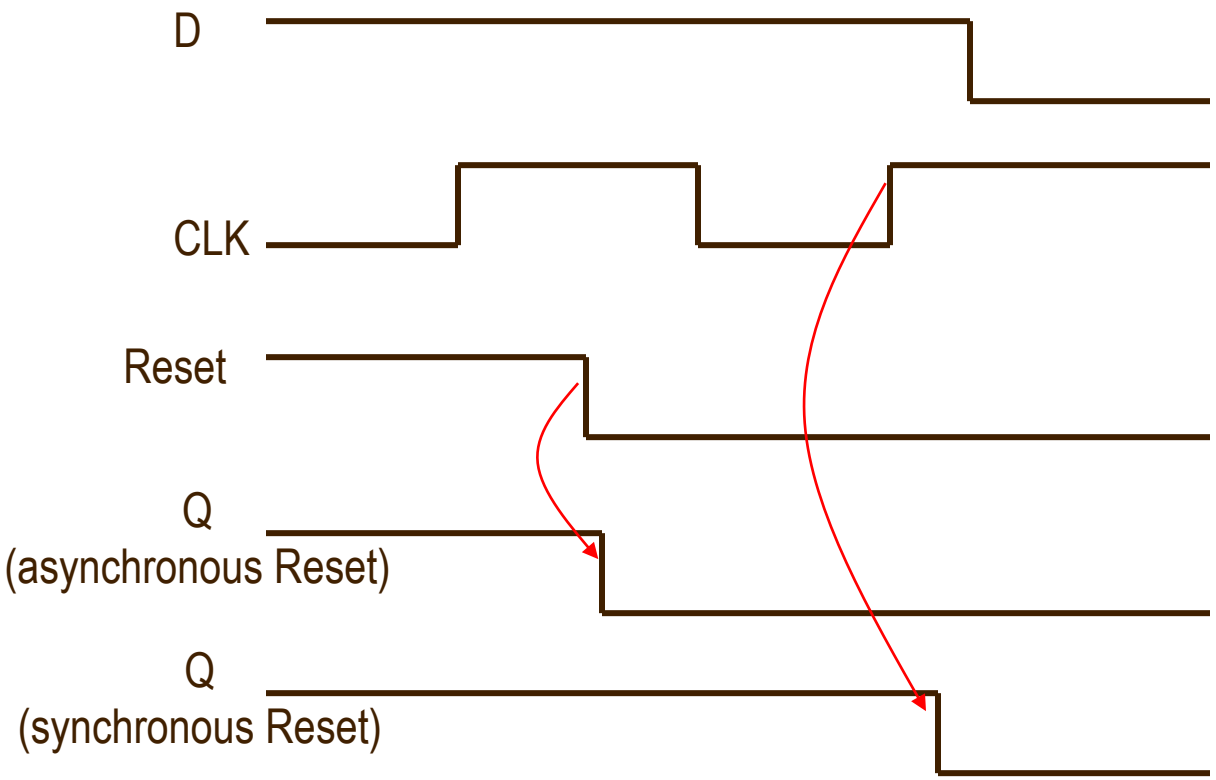


"Samples" D on rising edge of clock

Question 3

What is a difference between asynchronous Reset vs. synchronous Reset?

D Flip-Flop with Reset

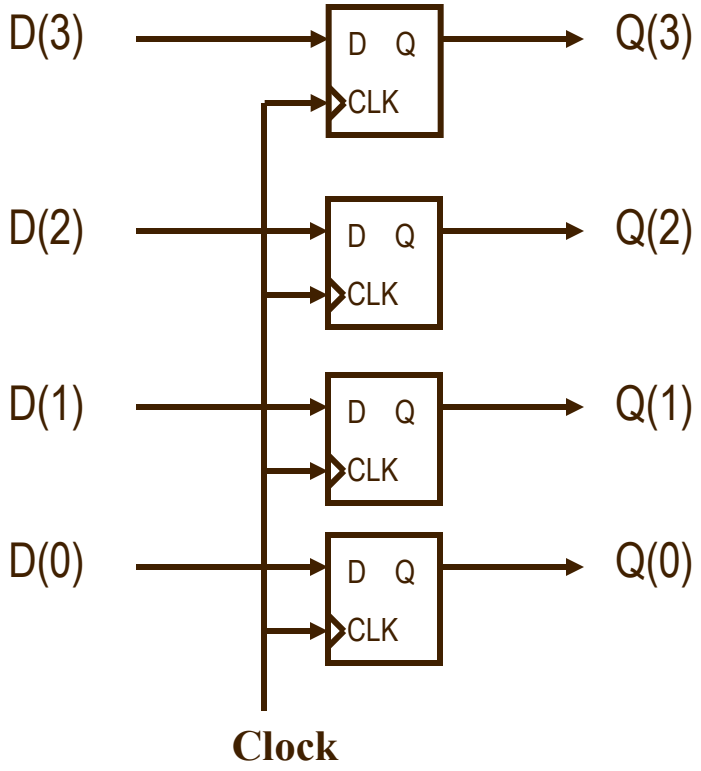


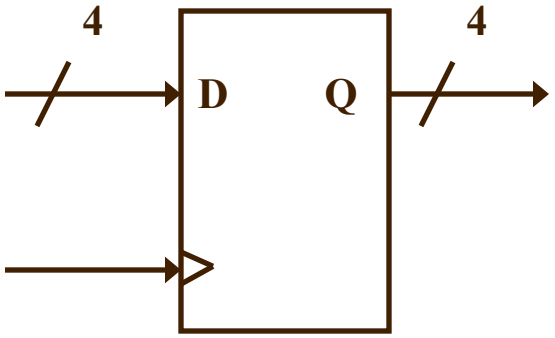
- Asynchronous active-low Reset: Q immediately clears to 0
- Synchronous active-low Reset: Q clears to 0 on rising-edge of clock

Question 4

What is a register?

Register



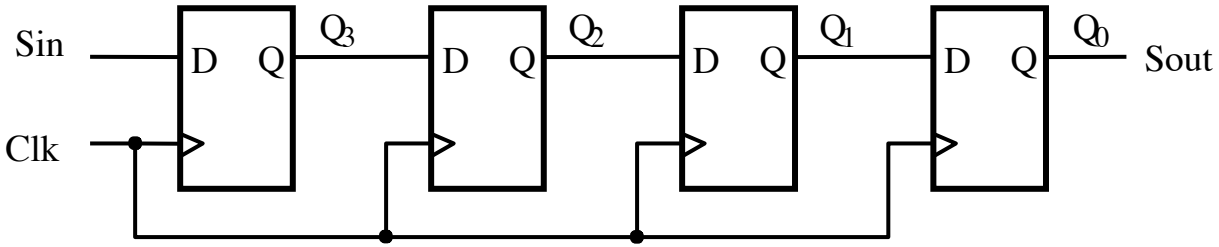


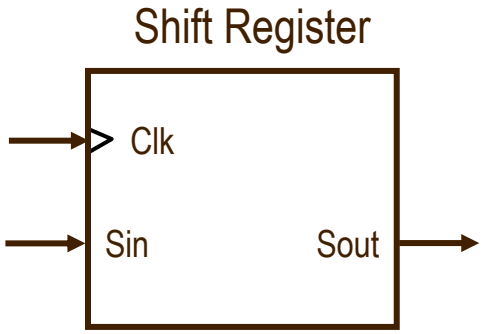
- In typical nomenclature, a register is a name for a collection of flip-flops used to hold a bus
- All flip-flops of a register share the same clock and control signals

Question 5

What is a functionality of a shift register?

Shift Register (shifting to the right)





	Sin	Q_3	Q_2	Q_1	Sout=Q_0
t_0	1	0	0	0	0
t_1	0	1	0	0	0
t_2	1	0	1	0	0
t_3	1	1	0	1	0
t_4	1	1	1	0	1
t_5	0	1	1	1	0
t_6	0	0	1	1	1
t_7	0	0	0	1	1

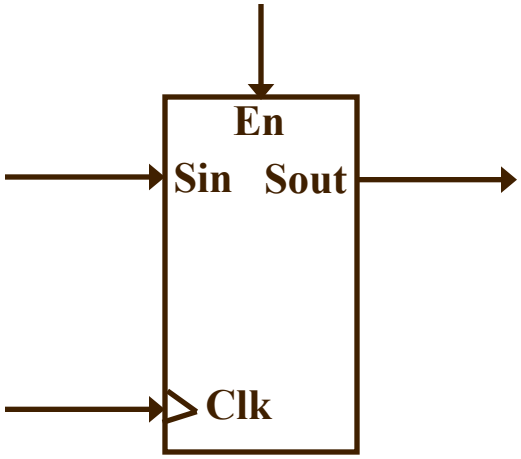
Question 6

Draw a symbol of a

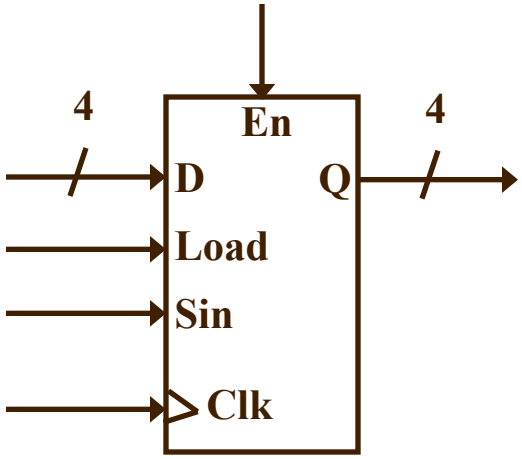
a. 4-bit Shift Register with Enable, shifting to the right, with Serial Input and Serial Output only
a. 4-bit Shift Register with Enable, shifting to the right, with Parallel Load, and Parallel Output

4-bit Shift Registers: symbols

a)



b)

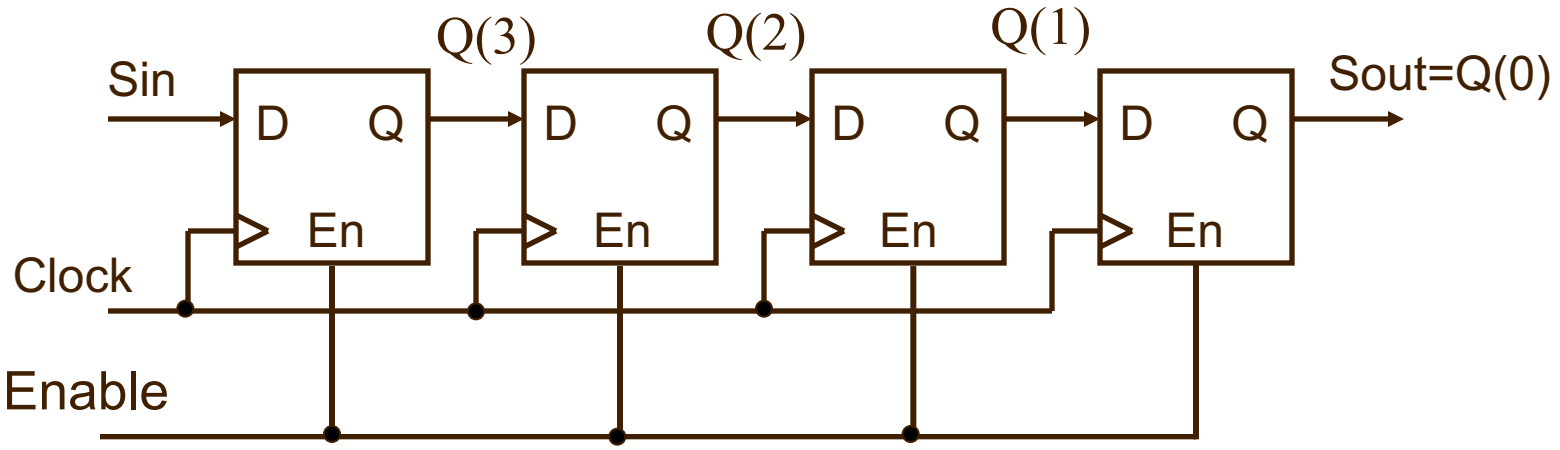


Question 7

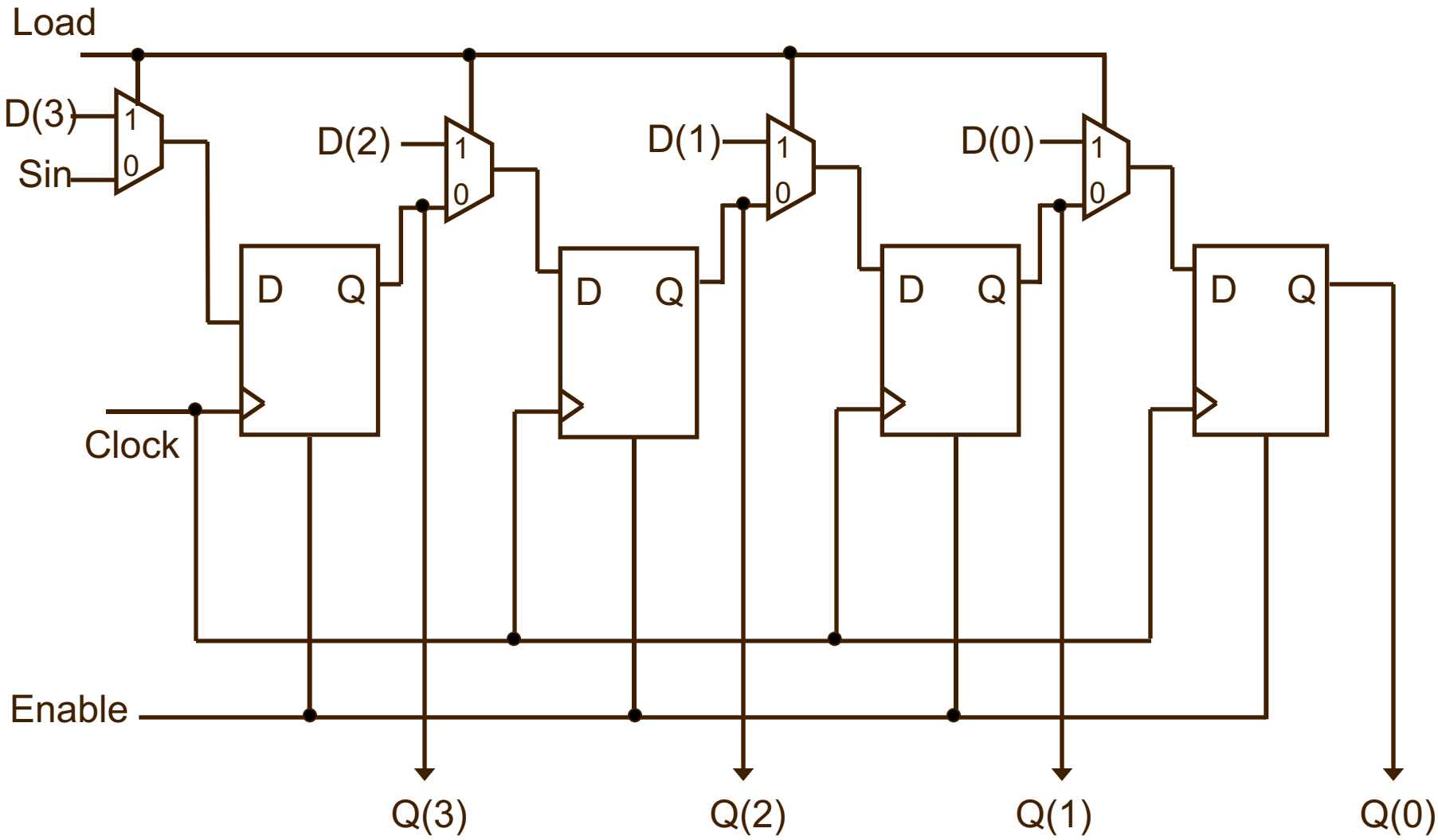
Draw a block diagram of a

a. 4-bit Shift Register with Enable, shifting to the right, with Serial Input and Serial Output only
a. 4-bit Shift Register with Enable, shifting to the right, with Parallel Load, and Parallel Output

Shift Register with Serial Input and Serial Output



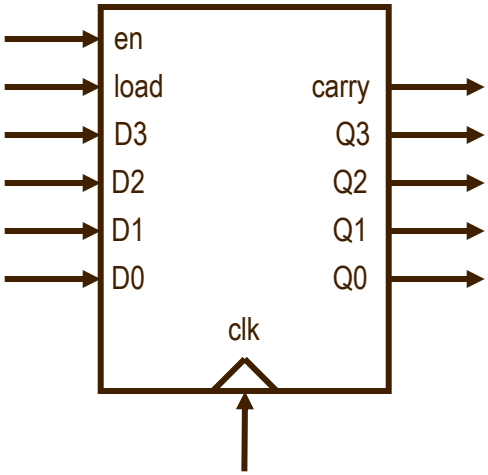
Shift Register with Parallel Load and Parallel Output



Question 8

What is the functionality of a counter?

Synchronous Up Counter

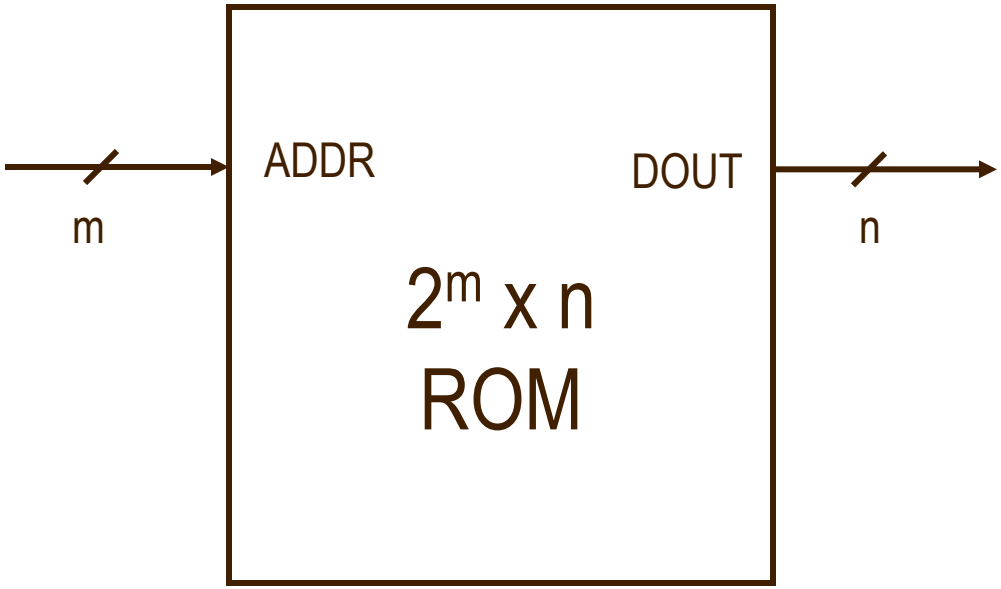


- enable (en) (synchronous): when high enables the counter, when low counter holds its value
- load (synchronous) : when load = 1, load the desired value into the counter
- output carry: indicates when the counter “rolls over”
- D3 downto D0, Q3 downto Q0 is how to interpret MSB to LSB

Question 9

What is a difference in terms of the required inputs and outputs between ROM and RAM of the same size (e.g., 2^m x n)?

Read Only Memory (ROM)



Random Access Memory (RAM)

- More efficient than registers for storing large amounts of data
- Can read and write to RAM
- Addressable memory
- RAM dimensions are:
  - (number of words) x (bits per word)
- Address is m bits, data is n bits
  - 2^m x n-bit RAM
- Example: address is 5 bits, data is 8 bits
  - 32 x 8 RAM
- Write Enable (WE)
  - When set, writing takes place at the next rising edge of the clock