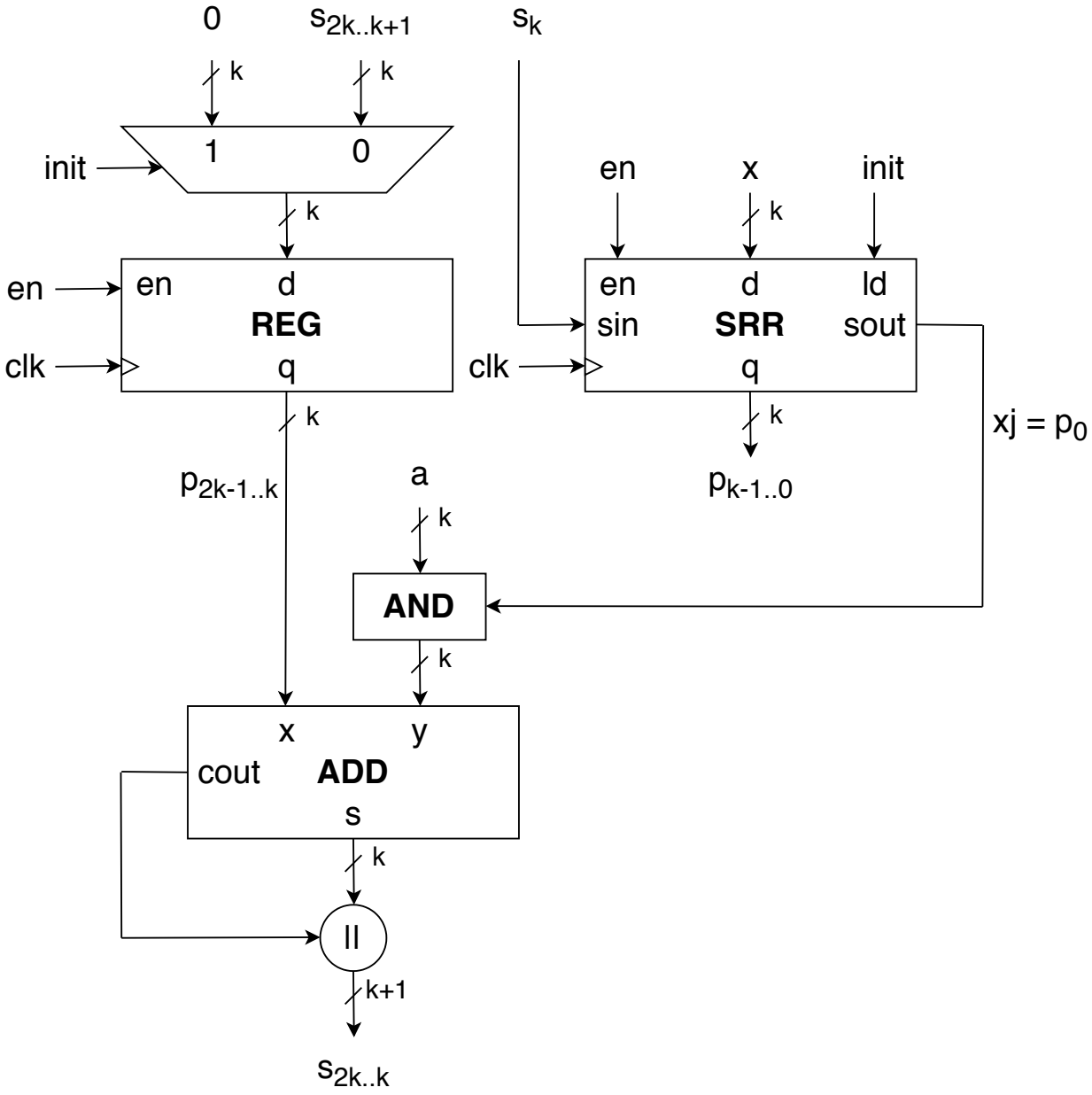
Timing Analysis – Class Exercise 1

Block diagram of a Sequential Unsigned Multiplier (SEQ_UMUL), implementing the Shift-and-Add algorithm is shown below:



Assume the following timing parameters of basic components:

$d_{REG} = d_{SRR} = d_{clk-q} = 1$ ns

$d_{AND} = 2$ ns

$d_{MUX} = 3$ ns

d_{ADD}(LSB(x), LSB(y)=>cout, k) $= 2 + 2 \cdot k$ ns

d_{ADD}(LSB(x), LSB(y)=>MSB(s), k) $= 4 + 2 \cdot k$ ns

$t_{setup} = 1$ ns.

Tasks:

Determine the critical path of this circuit for k=4.

Calculate:

1. Critical path delay
2. Minimum clock period
3. Maximum clock frequency
4. Slack for the target clock frequency equal to 50 MHz.

Solutions:

a)

Critical path delay (ns) =

$d_{SRR} + d_{AND} + d_{ADD}(LSB(x), LSB(y) \Rightarrow MSB(s), 4) + d_{MUX} + t_{setup} =$

$= 1 + 2 + 4 + 2 \cdot 4 + 3 + 1 =$

$= 19$

b) Minimum clock period = 19 ns

c) Maximum clock frequency = 1/19 ns = 1000/19 MHz = 52.6 MHz

d) Slack = 20 ns – 19 ns = 1 ns