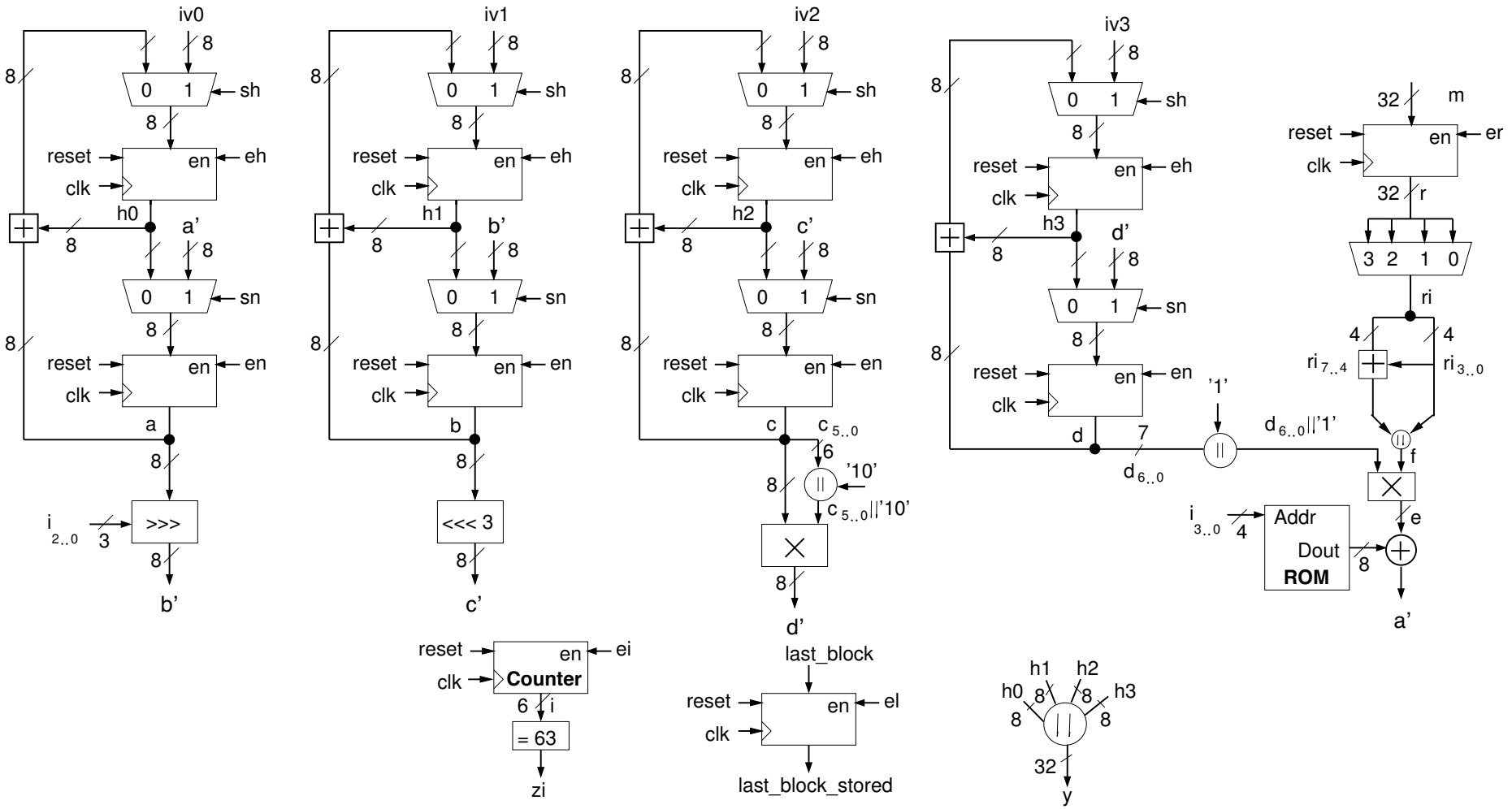
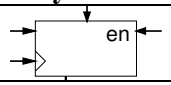
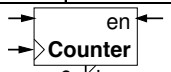
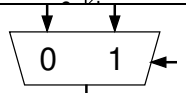
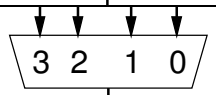
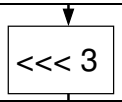
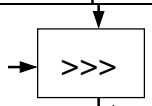
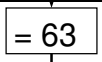
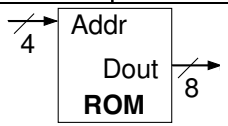
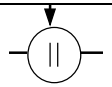
Timing Analysis – Class Exercise 2

Block diagram of a cryptographic hash function is shown below:



Please note that this block diagram contains connections by name!
For example, two 8-bit buses denoted by a' are assumed to be connected.

Assume the following notation and timing parameters of basic components:

Symbol	Logic/Arithmetic Component	Notation for a delay	Value of the delay
	Register	d_{REG}	1 ns
	Counter	d_{COUNT}	1 ns
	2-to-1 Multiplexer	d_{MUX2}	3 ns
	4-to-1 Multiplexer	d_{MUX4}	4 ns
	Adder modulo 2^8 (8-bit adder with carry out discarded) Adder modulo 2^4 (4-bit adder with carry out discarded)	d_{ADD8} d_{ADD4}	9 ns 5 ns
	Multiplier modulo 2^8 (8-bit multiplier with the MSB of the result discarded)	d_{MUL8}	15 ns
	Rotator by a constant	d_{CROT}	0 ns
	Variable rotator of an 8-bit input	d_{VROT}	9 ns
	6-bit Comparator with a constant	d_{COMP6}	7 ns
	Bitwise XOR	d_{XOR}	2 ns
	16x8 ROM	$d_{ROM16x8}$	5 ns
	Concatenation	d_{CONC}	0 ns

Additionally, assume that the setup time of all registers is t_{setup} = 1 ns.

Tasks:

Determine the critical path of this circuit and express it in terms of a sum of variables representing delays and setup times of all major components.

Calculate:

1. Critical path delay
2. Minimum clock period
3. Maximum clock frequency
4. Slack for the target clock frequency equal to 25 MHz.

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Solutions

Question:
Determine the critical path of this circuit and express it in terms of a sum of variables representing delays and setup times of all major components.

Answer:

$d_{critical\_path} = d_{REG} + d_{MUX4} + d_{ADD4} + d_{MUL8} + d_{XOR} + d_{MUX2} + t_{setup}$

Calculations:

1. **Critical path delay**

$d_{critical\_path} = (1 + 4 + 5 + 15 + 2 + 3 + 1)\ ns = 31\ ns$

2. **Minimum clock period**

$T_{clk} = d_{critical\_path} = 31\ ns$

3. **Maximum clock frequency**

$F_{clk} = 1/T_{clk} = 1/31\ ns = 1000/31\ MHz = 32.3\ MHz$

4. **Slack for the target clock frequency equal to 25 MHz.**

$Slack = 1/(25\ MHz) - 31\ ns = 40\ ns - 31\ ns = 9\ ns$