# ECE 545 Project Deliverables

Top-level folder:
`<First_Name>`

Second-level folders:
`1_assumptions`
`2_block_diagrams`
`3_interface`
`4_ASM_charts`
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`8_results`
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`10_bug_reports` [BONUS]

The recommended content of these folders is described below:

`1_assumptions`

A file containing the description of all assumptions (including possible simplifications) that you have made.

`2_block_diagrams`

Comments:

A. Please name and label all data buses and control signals in your circuit (at a minimum all inputs and outputs and all control and status signals that appear at the interface between the Controller and Datapath). In order to support debugging of your code, I would also suggest naming all intermediate buses and nodes of the Datapath that appear as signals in your VHDL code.
B. All diagrams must be submitted in
PDF.

You can draw diagrams in a graphical editor of your choice (e.g., Dia, Xfig, MS Visio).

You can also submit scanned versions of handwritten block diagrams.

C. In the file: `hierarchy.txt`, please include the list of all block diagram files, starting from the block diagram of your top-level unit down to the block diagrams of your lowest-level components.

*D.* BONUS: The complete editable versions of block diagrams prepared using a graphical editor will be rewarded with bonus points. *Please note that you would still need to submit PDF versions.*

`3_interface`

`A_top_level`
`B_division`

Comments:

Re: `A_top_level`

This is a top-level interface of your circuit.

Draw a diagram of your interface, and describe the meanings of all inputs and outputs.

Re: `B_division`

Interface with the division into the Datapath and Controller.

`4_ASM_charts`

Comments:

A. If more than one FSM is used, please include a block diagram illustrating communication among all FSMs.

B. As a minimum, please include scans of your handwritten ASM charts and the controller block diagram in the PDF format.

*C.* BONUS: The complete editable versions of ASM charts prepared using a graphical editor will be awarded with bonus points. *Please note that you would still need to submit PDF versions.*

`5_source_codes`

Comments:
A. Please include all synthesizable VHDL codes of the Datapath, the Controller, and the Top-Level Circuit.

B. Please include also a file `source_list.txt` listing all files in the order they should be synthesized (bottom-up).

`6_verification`

**[THIS PART IS EXTREMELY IMPORTANT AND MAY DETERMINE YOUR FINAL GRADE]**

In this folder include:

A. All testbenches used to verify your circuit operation at various levels of hierarchy.

B. All programs (in C, Matlab, or other languages) you have used to generate test vectors.

C. All test vector files you have used for verification and debugging.

D. Report describing:

- your strategy for verification: order of tests and testbenches used, source and format of test vectors

- highest level entity verified for functional correctness and the results of its verification

  If the result of any verification was negative (i.e., your circuit did not operate as expected), please describe incorrect behavior and try to explain the possible sources of errors.

- verification of lower-level entities (optional if the top-level unit was verified to work correctly):

  - Name of an entity
  - Testbench used for verification
  - Test vectors and their source
  - Result of verification, correct or incorrect behavior
  - Possible sources of errors.

`7_timing_analysis`

Comments:
A. In the file
`timing.pdf`
please provide the exact formulas for

a. Execution time as a function of the input size, m, expressed in clock cycles.

b. Latency = Execution time for a single input, expressed in clock cycles.

c. Time between two consecutive inputs or outputs (in clock cycles).

d. Throughput for short messages as a function of the clock period, T, and the input size, m (calculated as a ratio of the total input size and the total execution time).

e. Throughput for long messages as a function of the clock period, T (calculated as a ratio of the input block size and the time between inputting two consecutive input blocks).

B. Please do your best to confirm the execution time of your circuit through simulation.

Please clearly indicate in `timing.pdf`, which formulas in your report have been confirmed through functional simulation, and which circuit was used in these simulations (entire core, datapath, other?).

`8_results`

Please submit a document containing the following results for

a. Xilinx Spartan-6
b. Xilinx Virtex-6
c. Altera Stratix IV [BONUS]

A. resource utilization

B. numerical values of the following timing parameters
    a. Minimum Latency
    b. Maximum Throughput
    c. Maximum Throughput/Area
   based on the minimum clock period after placing and routing.

C. Excel graphs and charts summarizing results for all FPGA families you attempted

D. analysis of the obtained results; your observations and conclusions.

`9_benchmarking` [BONUS]

Divide this folder into subdirectories corresponding to each individual family:

a. Xilinx Spartan-6
b. Xilinx Virtex-6
c. Altera Stratix-IV.

For each run of ATHENa please include only:

- `report_option.txt`
- `report_execution_time.txt`
- `report_timing.txt`
- `report_resource_utilization.txt`
- `report_summary.txt`
- `athena_log.txt`, and
- the `config` subfolder.

In the folder

`summary`

please include the report file

`benchmarking.pdf`

containing

- list of optimization strategies (ATHENa applications) used to obtain best results

- Excel graphs and charts summarizing all results

- analysis of the obtained results; your observations and conclusions.

`10_bug_reports` [BONUS]

In this folder, please include the following subfolders

```
1_articles
2_ATHENa
3_Other
```

Each bug report should be placed in a separate subfolder of these directories, and named:

`bug_<n>_mm_dd`, where
`mm_dd` represents the month and day when a given problem was discovered, and
`<n>` is a unique bug number.

For each bug you report, please include short description.

In
`1_articles`
please describe all mistakes you have found in articles or textbooks describing an algorithm assigned to you (or its implementation).

These mistakes can include mistakes in the pseudocode, block diagrams, figures, tables, explanations, etc.

In
`2_ATHENa`
please include all information necessary to recreate the same problem (in particular, the version of ATHENa used, design.config.txt, source files, versions of Xilinx and Altera tools used, simulator used, etc.).