SORTING Circuit
Specification

Function

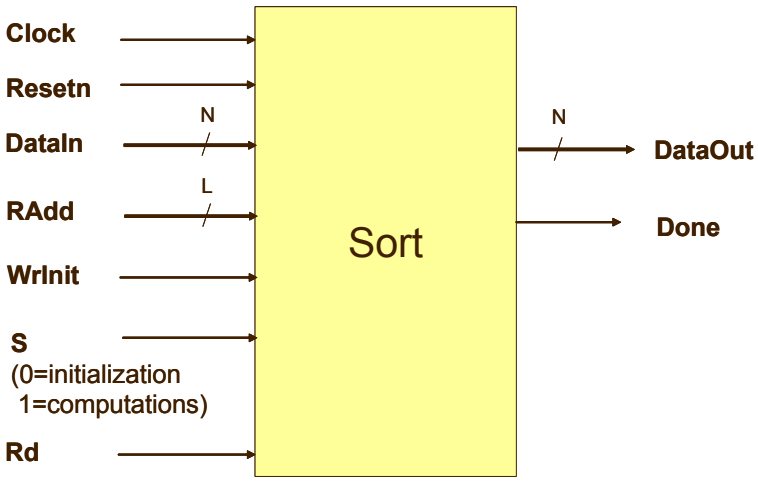
Design a circuit capable of sorting 2^L N-bit numbers.

Optimization

Optimize your circuit for the minimum total execution time. When choosing between two circuits with the same or very similar execution time, give preference to the circuit with the smaller area.

Interface

Assume the following interface to your circuit:



Port	Width	Meaning
clk	1	System clock
Resetn	1	System reset – clears internal registers. Active low.
DataIn	N	Input data bus
RAdd	L	Address of the internal memory where input data is stored
WrInit	1	Synchronous write control signal
s	1	Operating mode: 0 = initialization, 1 = computations.
Rd	1	Read enable. 0 = high impedance on the output bus, 1 = valid output on the output data bus.
DataOut	N	Output data bus used to read results
Done	1	Asserted when all results are ready

Task 1

Develop a pseudocode describing a selected sorting algorithm.

Task 2

Draw a block diagram of the Datapath of the SORTING circuit. Use medium complexity components corresponding to the operations used in the pseudocode.
Clearly specify

- **names, widths and directions of all buses**
- **names, widths and directions of all inputs and outputs of the logic components.**

Minimize the number of control signals to be generated by Control Unit.

Mark the most likely critical path in your circuit.

Task 3

Draw an interface of the SORTING circuit with the division into Datapath and Controller.