ECE 545
Lecture 8

Timing Analysis

Required reading

- P. Chu, *RTL Hardware Design using VHDL*

Chapter 8.6 Timing Analysis of a Synchronous Sequential Circuit

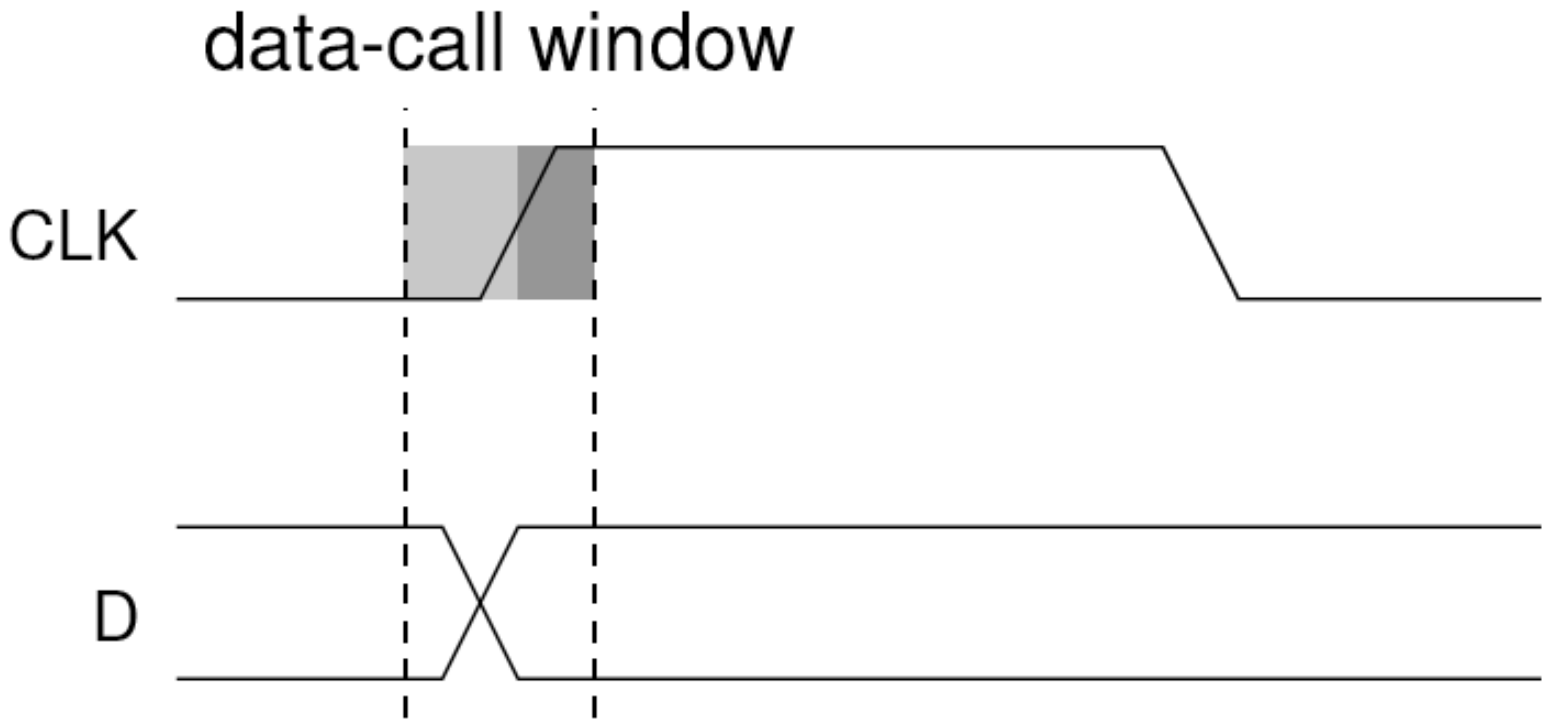
Chapter 16.1 Overview of a Clock Distribution Network

Chapter 16.2 Timing Analysis with Clock Skew

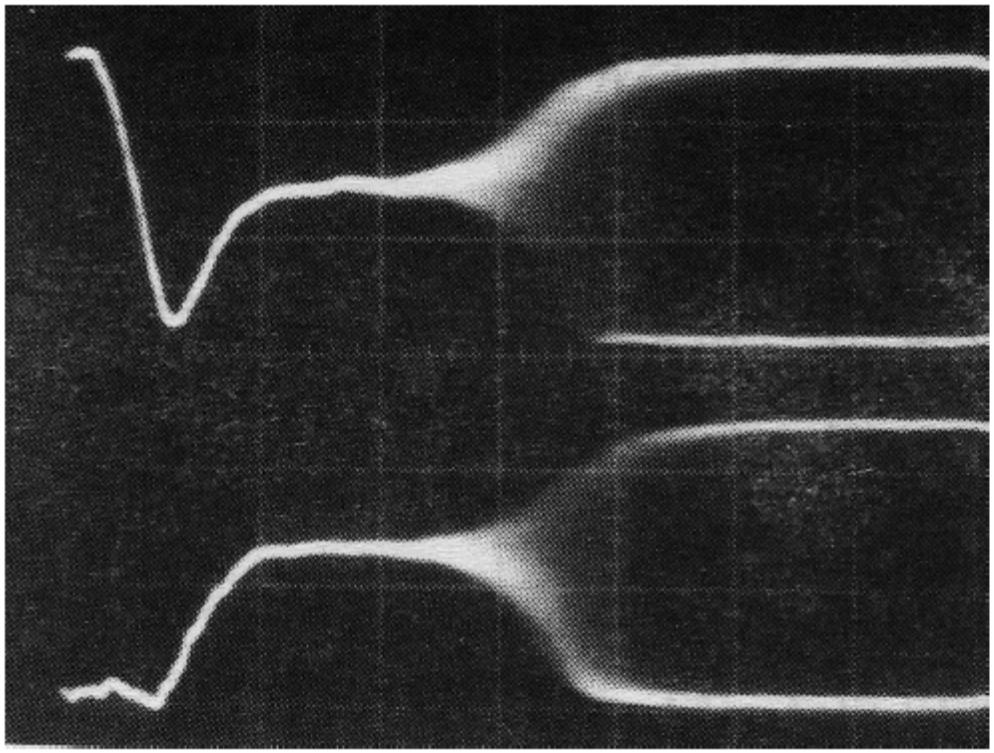


Hold & Setup Time
Metastability

Violation of Hold or Setup Time



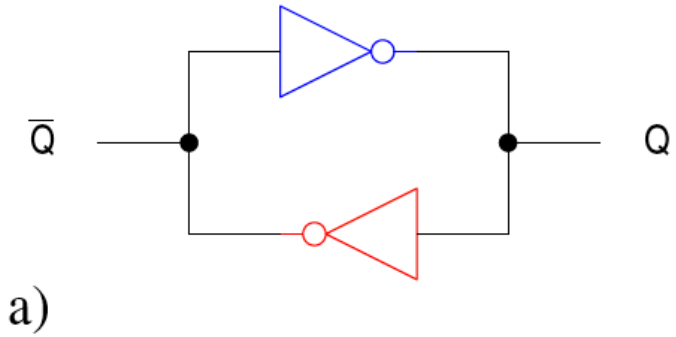
Response of a Flip-Flop to Timing Violation



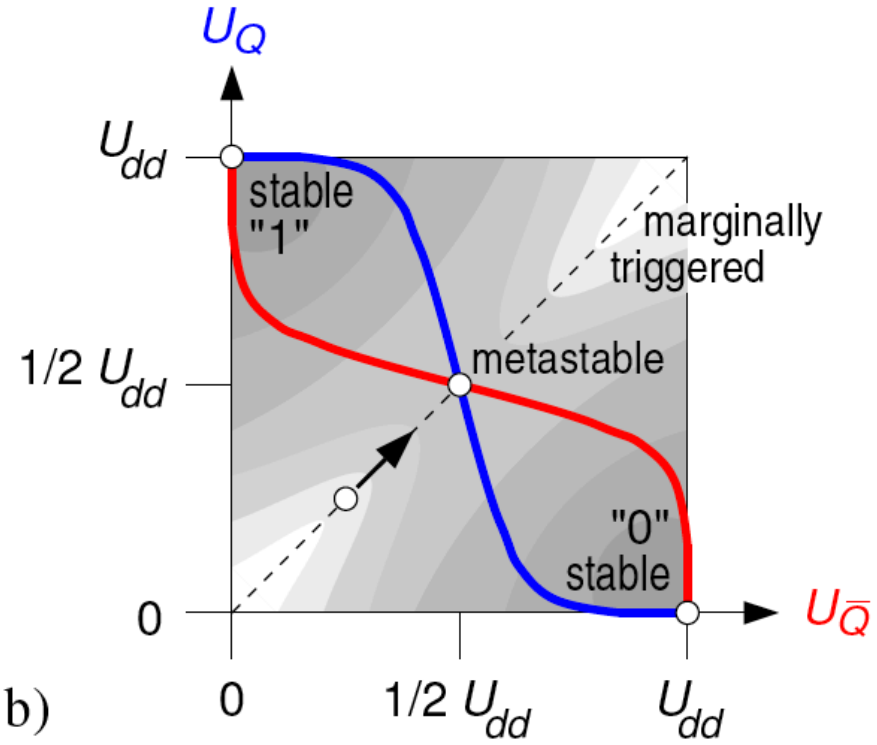
There exists a third and unstable point of equilibrium between the two stable states representing the binary states 0 and 1 respectively.

Points of Equilibrium in Flip-Flops and Latches

- Today's latches and flip-flops are inherently analog networks.
- Data retention is obtained from closed feedback loops built from two inverting amplifiers.

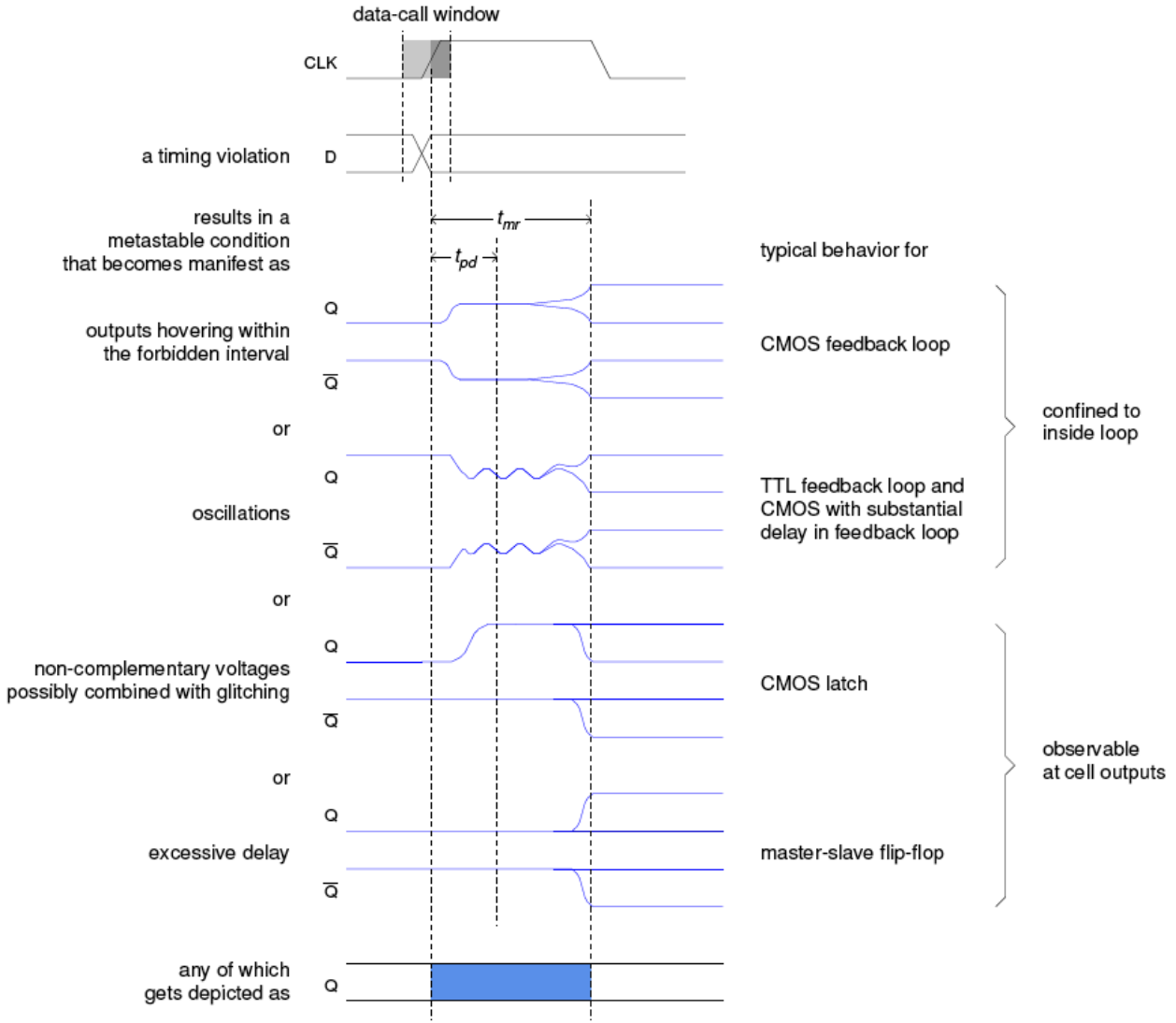


a)

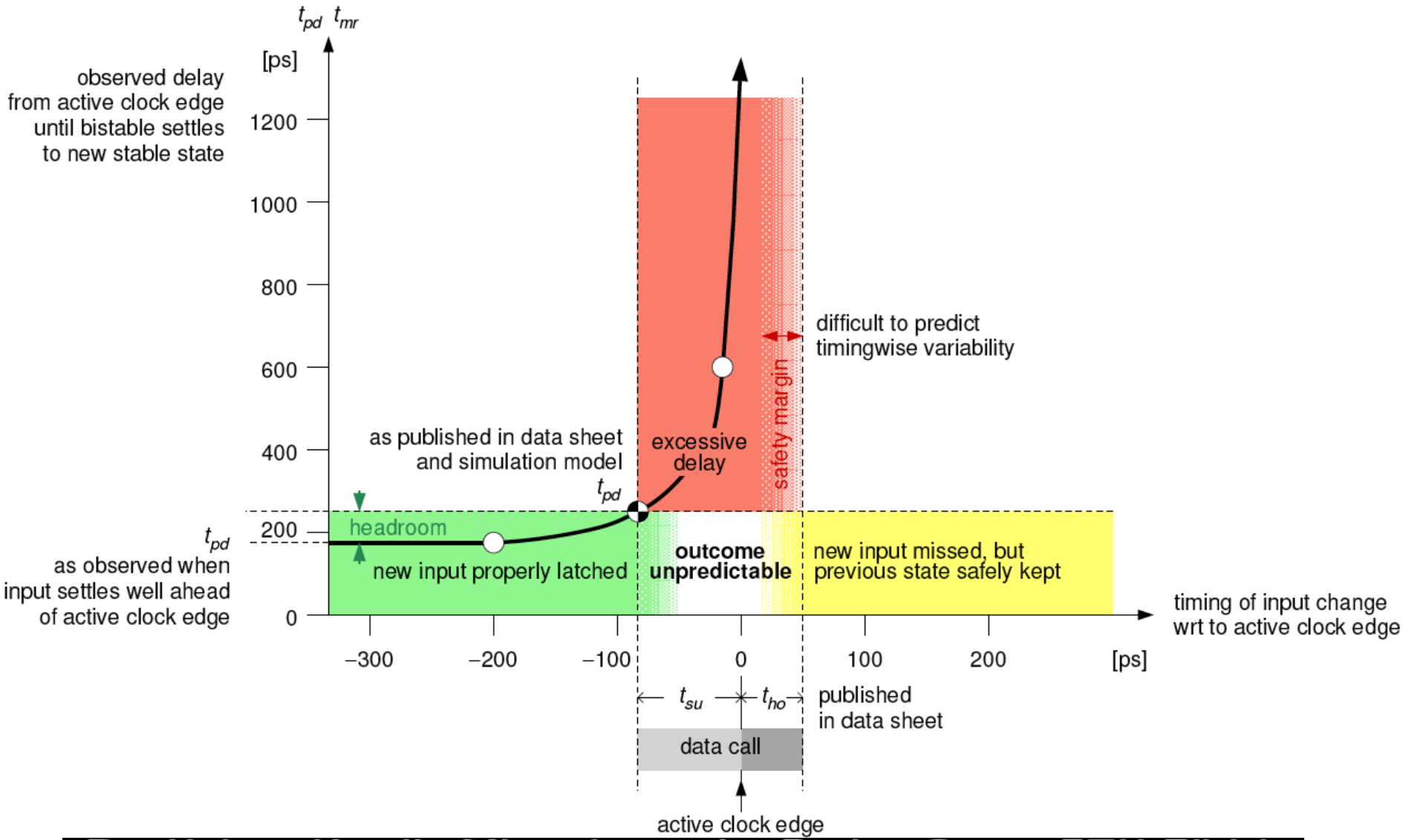


b)

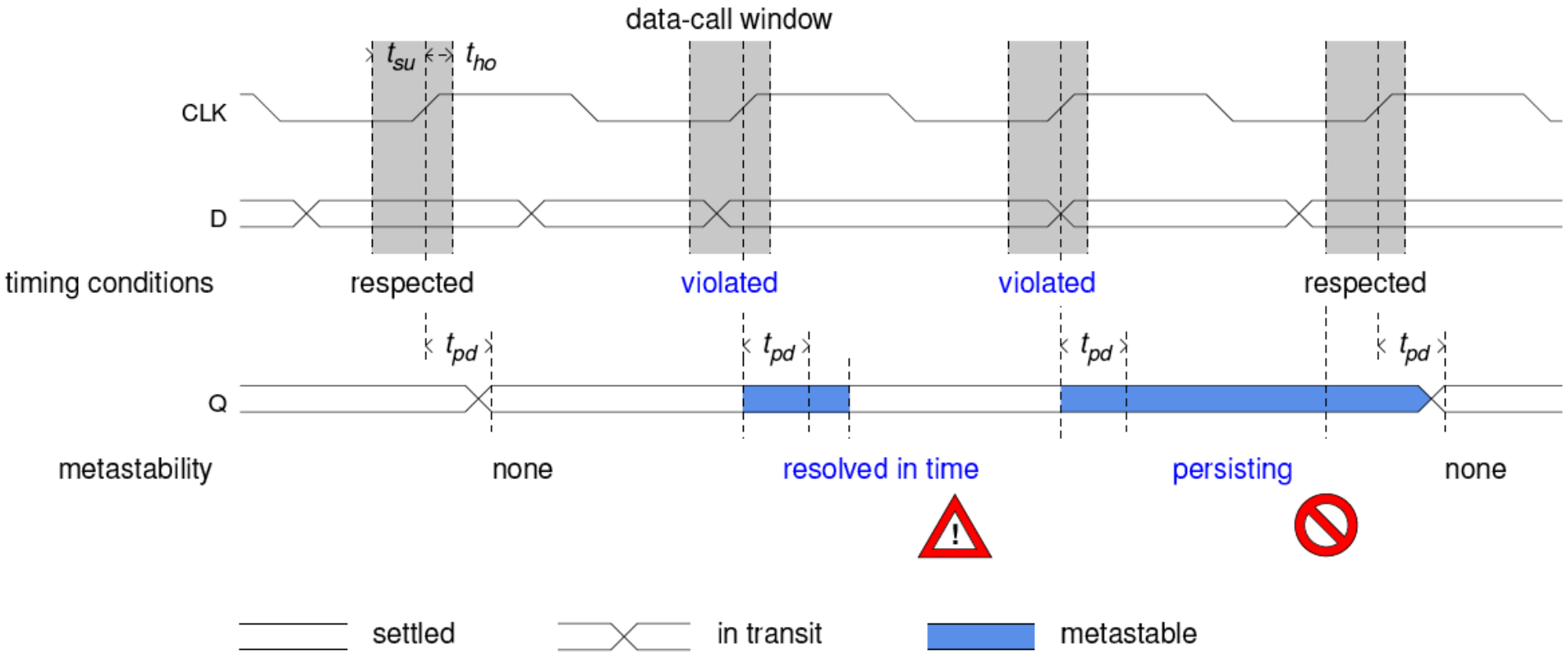
Patterns of Metastable Behavior



Response to Timing Violation



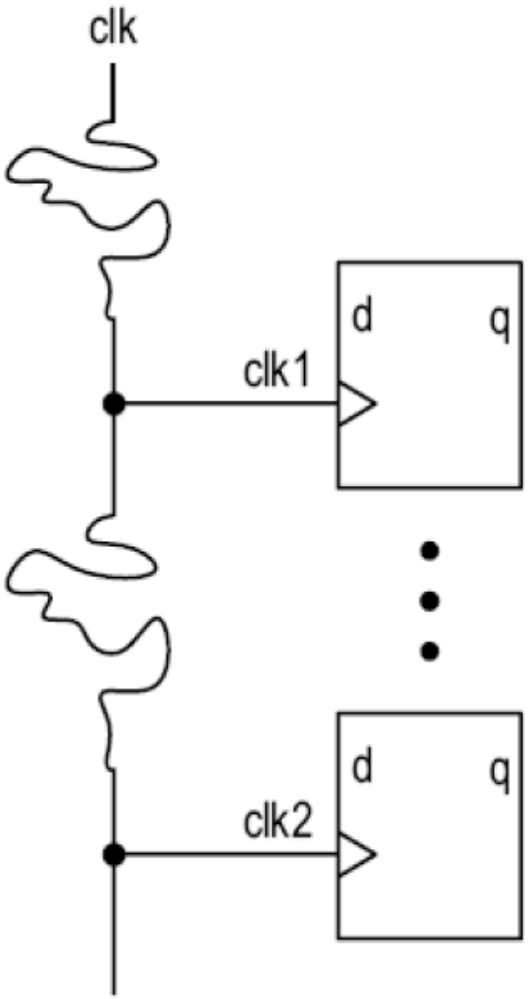
Impact on Downstream Circuitry

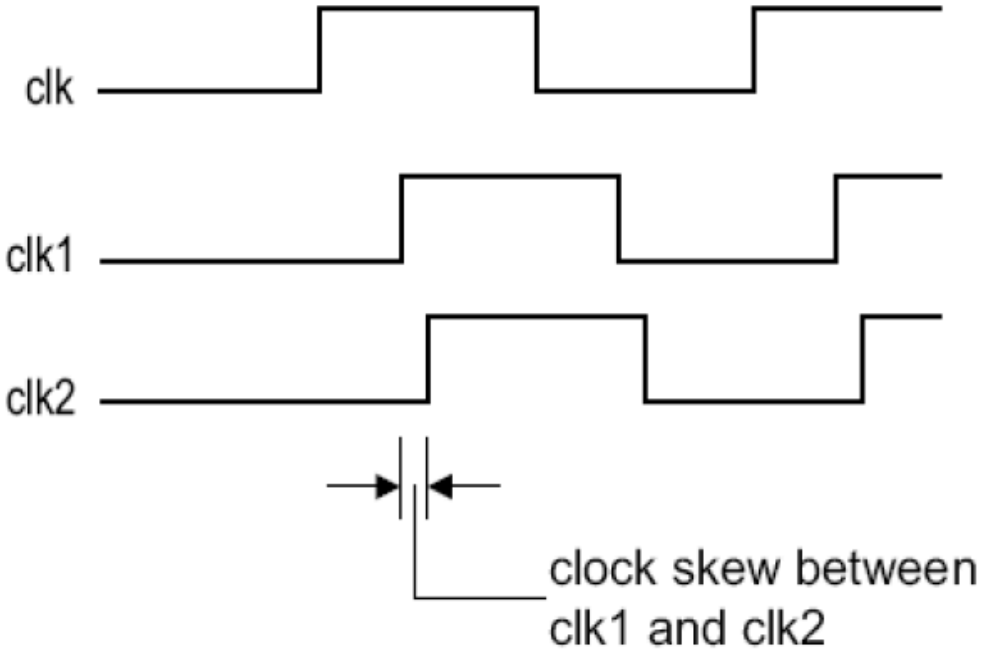




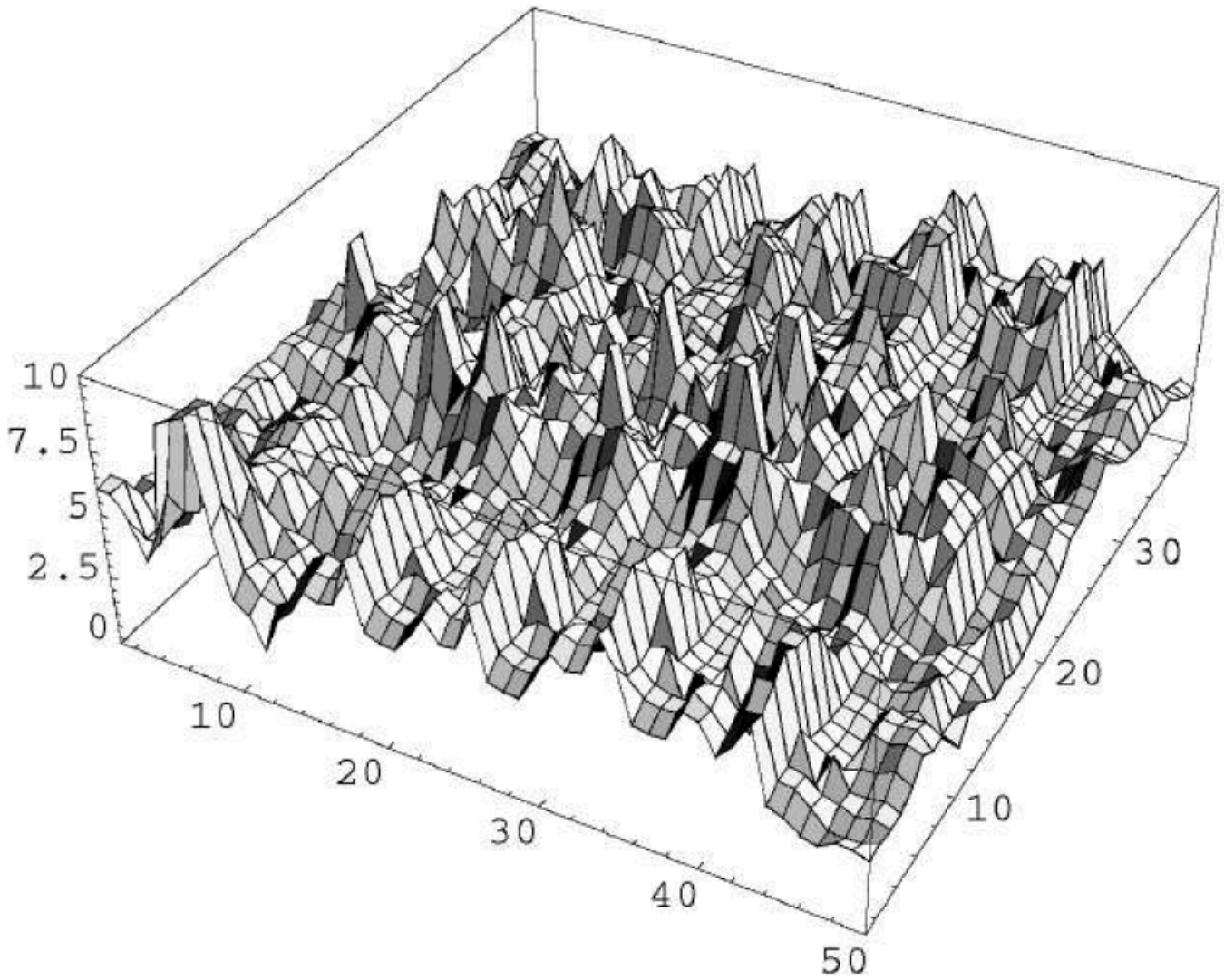
Clock Skew

Clock Skew

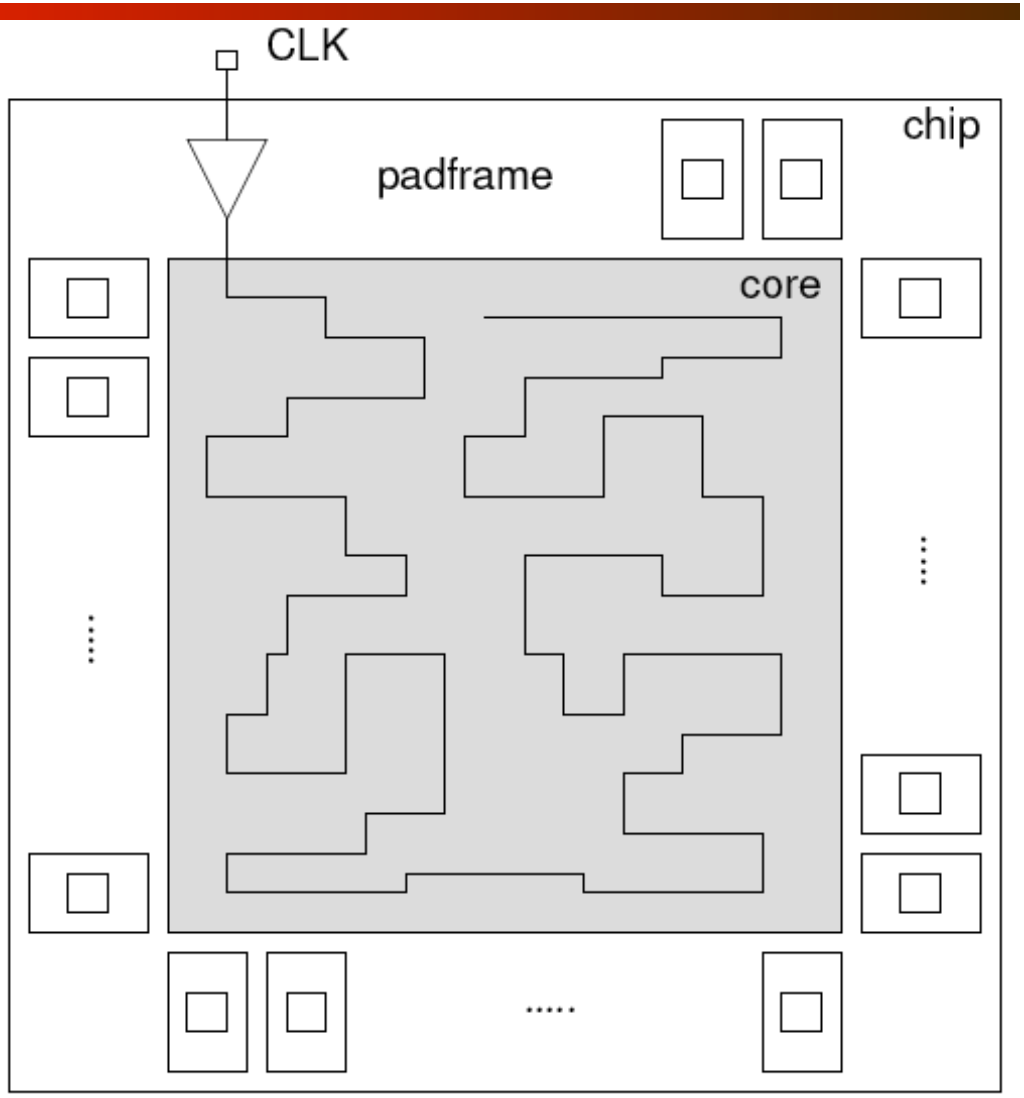

clk
clk1
d
q
clk2
d
q


clk
clk1
clk2
clock skew between
clk1 and clk2

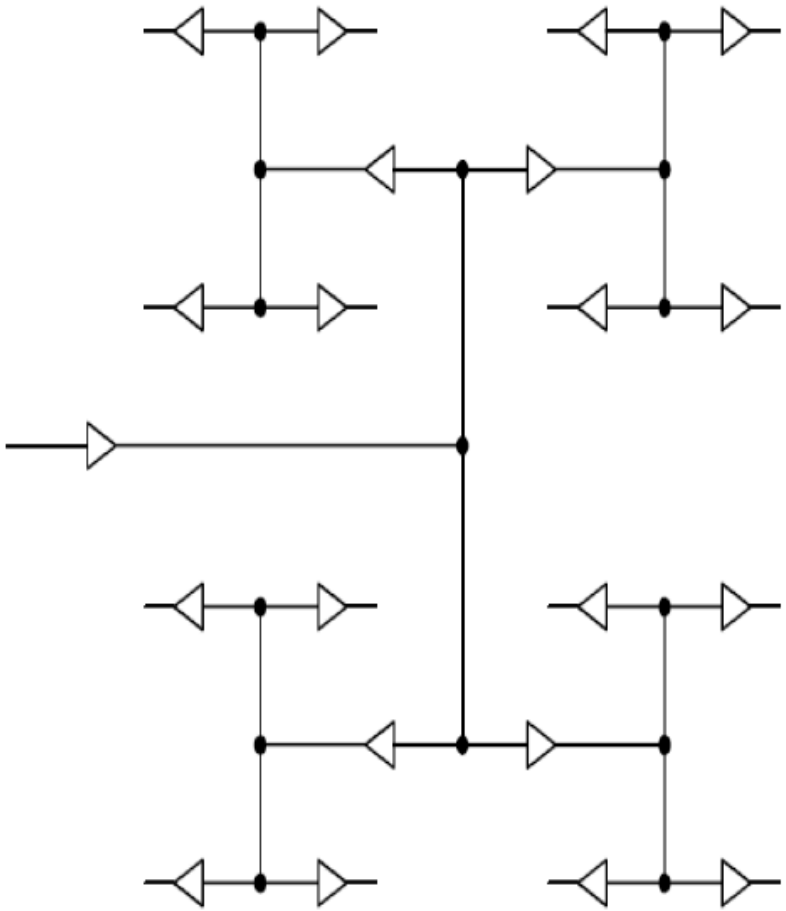
Clock Skew Map for a Cell Processor



Incorrect Clock Tree Layout – Narrow Meander



Optimized Clock Tree Layout – H Tree



Clock Skew - Summary

- Clock skew normally has negative impact on synchronous sequential circuit
- Effect on setup time constraint: require to increase clock period (i.e., reduce clock rate)
- Effect on hold time constraint: may introduce hold time violation
  - Can only be fixed during physical synthesis: re-route clock; re-place register and comb logic; add artificial delay logic
- Skew within 10% of clock period tolerable