

ECE 545

Remaining Tasks

Grading Scheme

- **Midterm Exam - 20%**
- **Homework - 15%**
- **Final Exam - 30%**
- **Project - 35%**

Final exam

- ✓ 2 hours 45 minutes
- ✓ in class
- ✓ design-oriented
- ✓ open-books, open-notes
- ✓ practice exams available on the web

Date:

Thursday, December 12, 4:30-7:15pm

Typical Exam Problems

1. (pseudocode, interface) => block diagram
2. interface (w/ division into Datapath and Controller)
3. (pseudocode, interface, block diagram) =>
   ASM chart
4. actions => control signals
5. timing waveforms based on ASM charts & inputs
6. timing analysis (execution time, latency, throughput, critical path, clock skew)
7. VHDL code of controllers
8. memories in Xilinx FPGAs
9. combinational and sequential circuit building blocks

Project

4th Progress Report:

Sunday, December 8, 11:59 PM

Final Deadline (firm):

Sunday, December 15, 11:59 PM