

ECE 545

Remaining Tasks

Grading Scheme

- **Homework - 15%**
- **Midterm Exam - 20%**
- **Final Exam - 30%**
- **Project - 35%**
- **Class Activity - Bonus 5%**

Bonus Points for Class Activity

- **Based on class exercises during lecture**
- **"Small" points earned each week**
- **Up to 5 "big" bonus points**
- **Scaled based on the performance of the best student**

For example:

	Small points	Big points
1. Alice	40	5
2. Bob	36	4.5
…	…	…
28. Charlie	8	1

Final exam

- ✓ 2 hours 45 minutes
- ✓ in class
- ✓ design-oriented
- ✓ open-books, cheat sheet
- ✓ practice exams available on the web

Date:

Thursday, December 14, 4:30-7:15pm

Typical Exam Problems

1. (pseudocode, interface) => block diagram
2. interface (w/ division into Datapath and Controller)
3. (pseudocode, interface, block diagram) => ASM chart
4. actions => control signals
5. timing waveforms based on ASM charts & inputs
6. timing analysis (execution time, latency, throughput, critical path, clock skew)
7. VHDL code of controllers
8. memories in Xilinx FPGAs
9. combinational and sequential circuit building blocks

Project Deadline

Sunday, December 17th, 11:59 PM