ECE 545
Lecture 13

Timing Analysis

Required reading

- P. Chu, *RTL Hardware Design using VHDL*

Chapter 8.6 Timing Analysis of a Synchronous Sequential Circuit

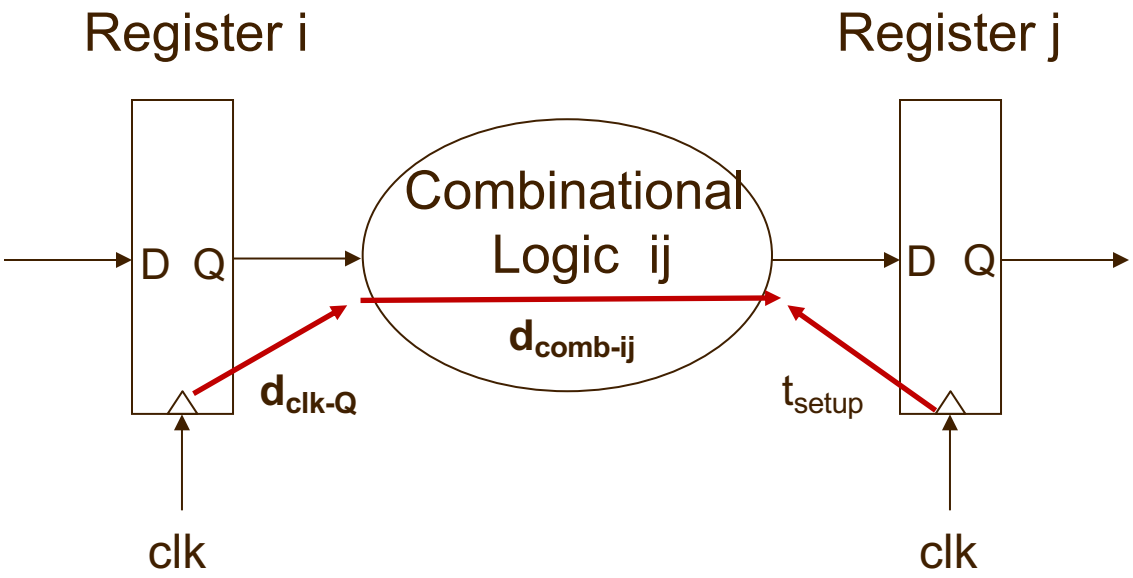
Chapter 16.1 Overview of a Clock Distribution Network

Chapter 16.2 Timing Analysis with Clock Skew

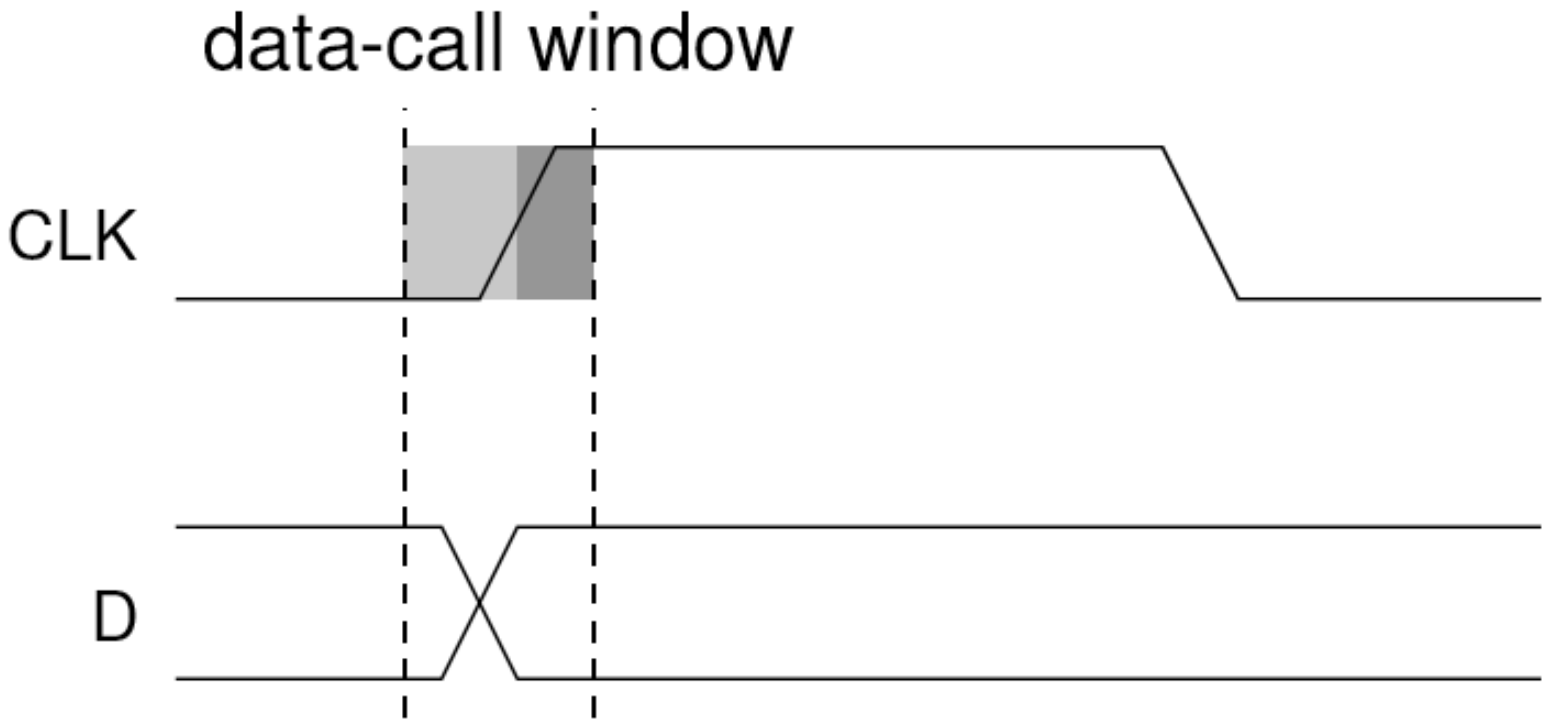


Hold & Setup Time

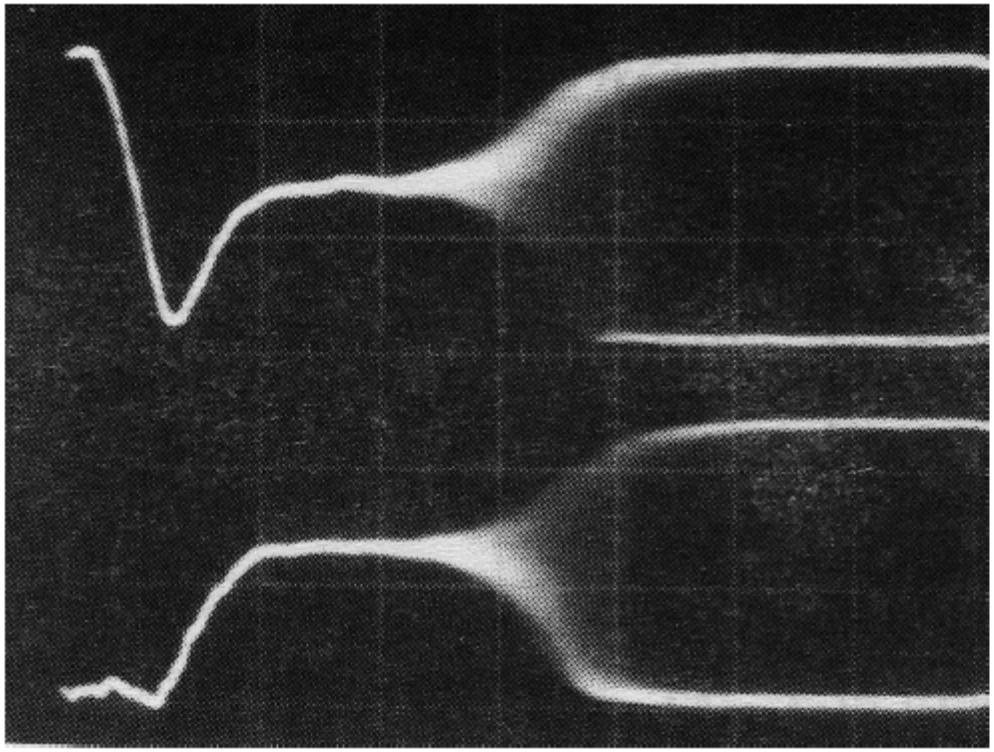
Path Between Two Adjacent Registers



Violation of Hold or Setup Time

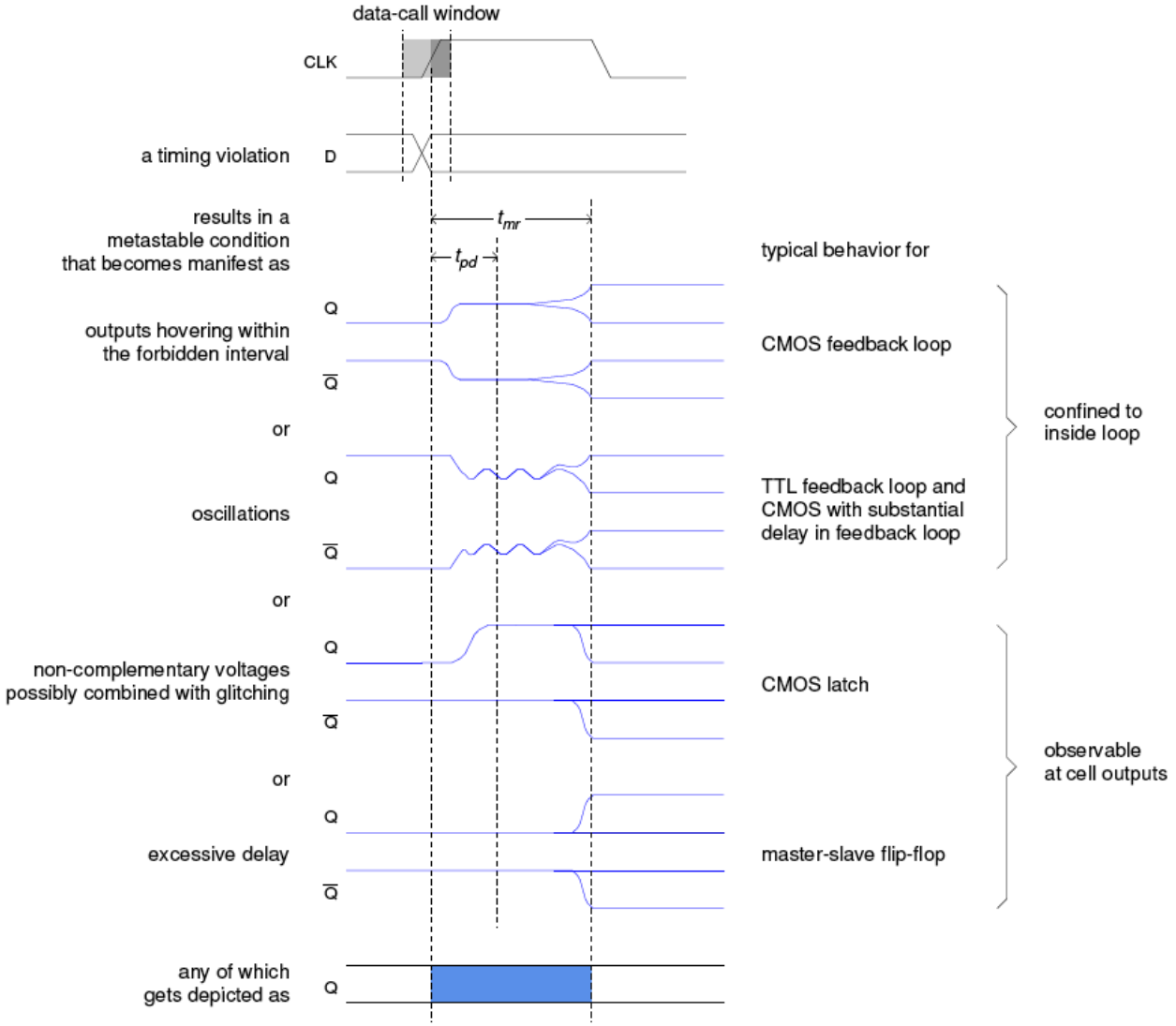


Response of a Flip-Flop to Timing Violation

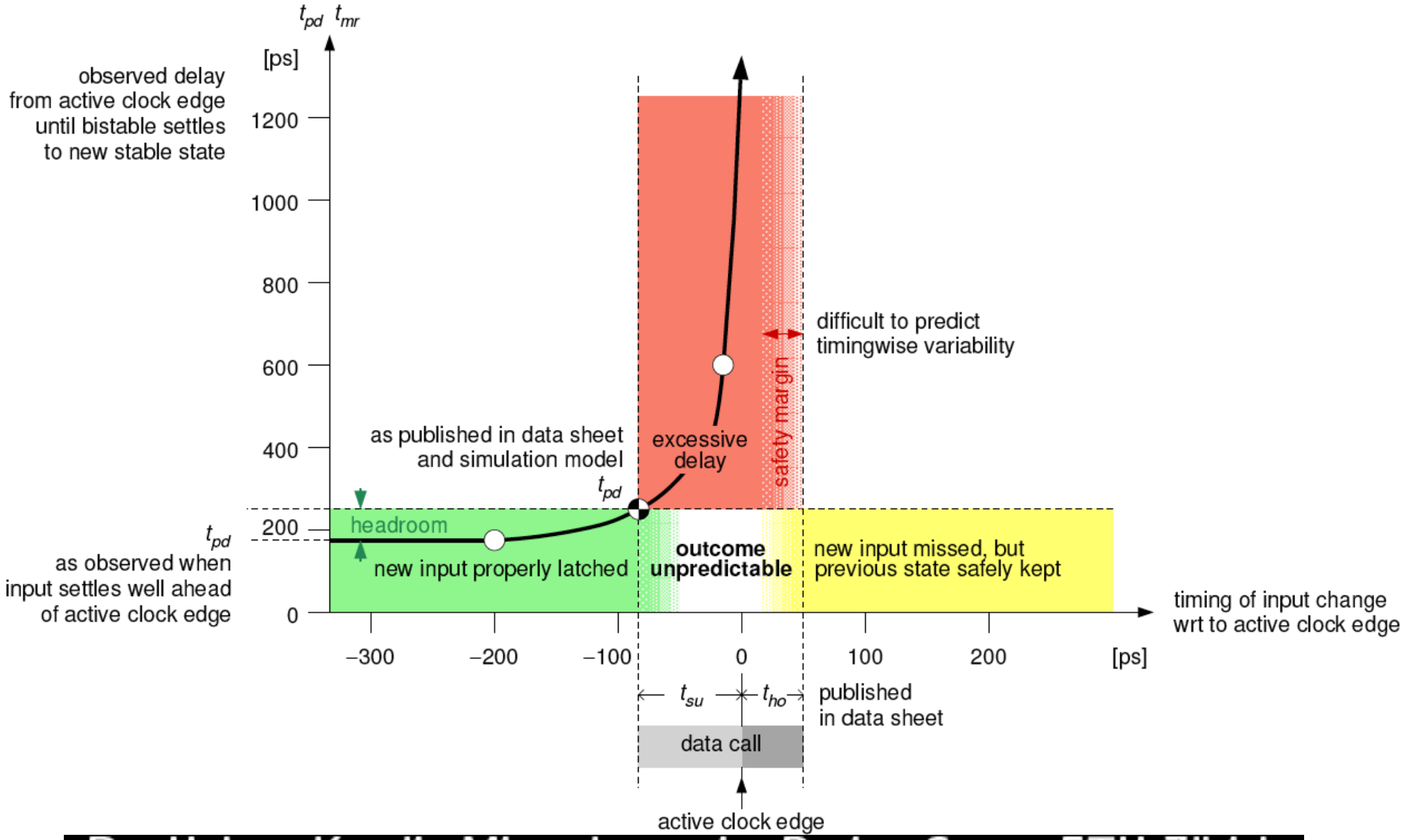


There exists a third and unstable point of equilibrium between the two stable states representing the binary states 0 and 1 respectively.

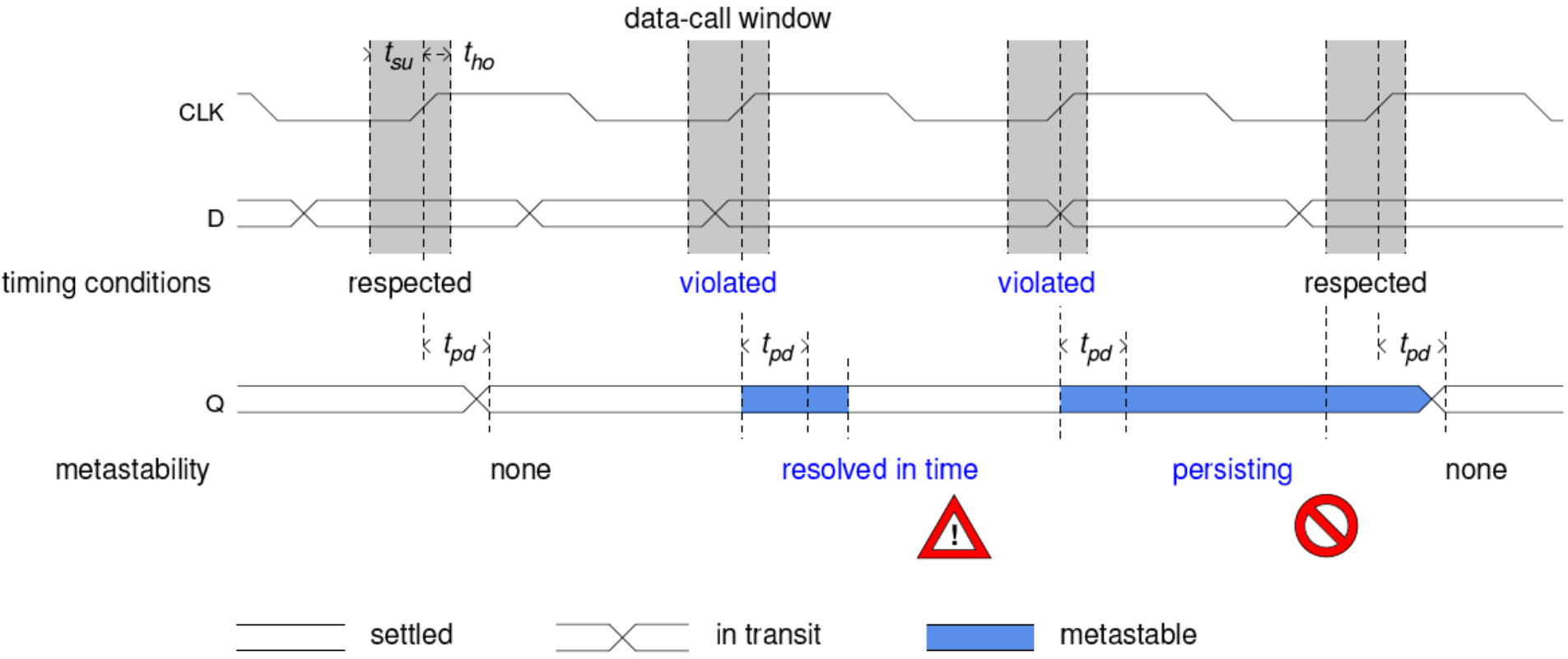
Patterns of Metastable Behavior



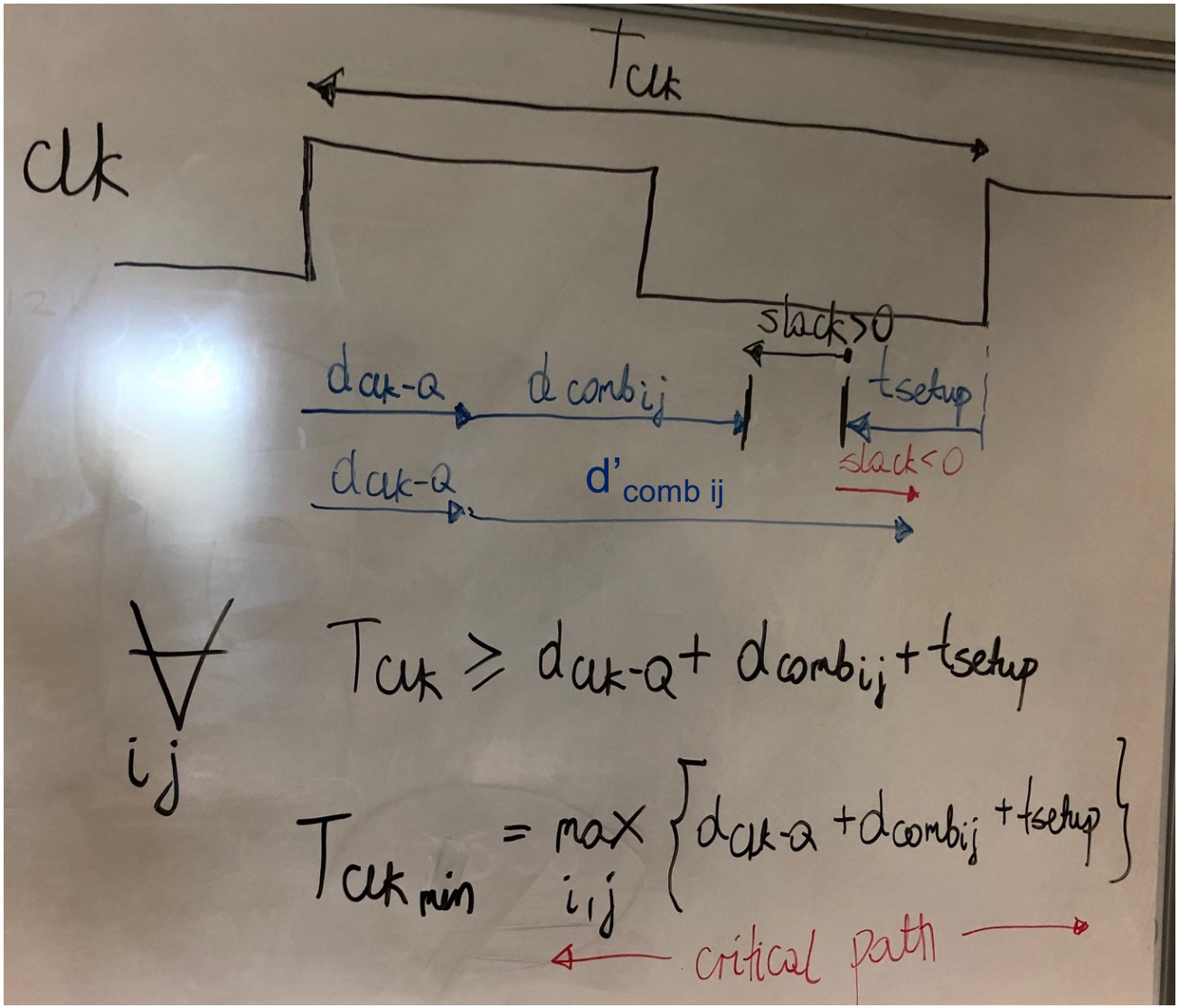
Response to Timing Violation



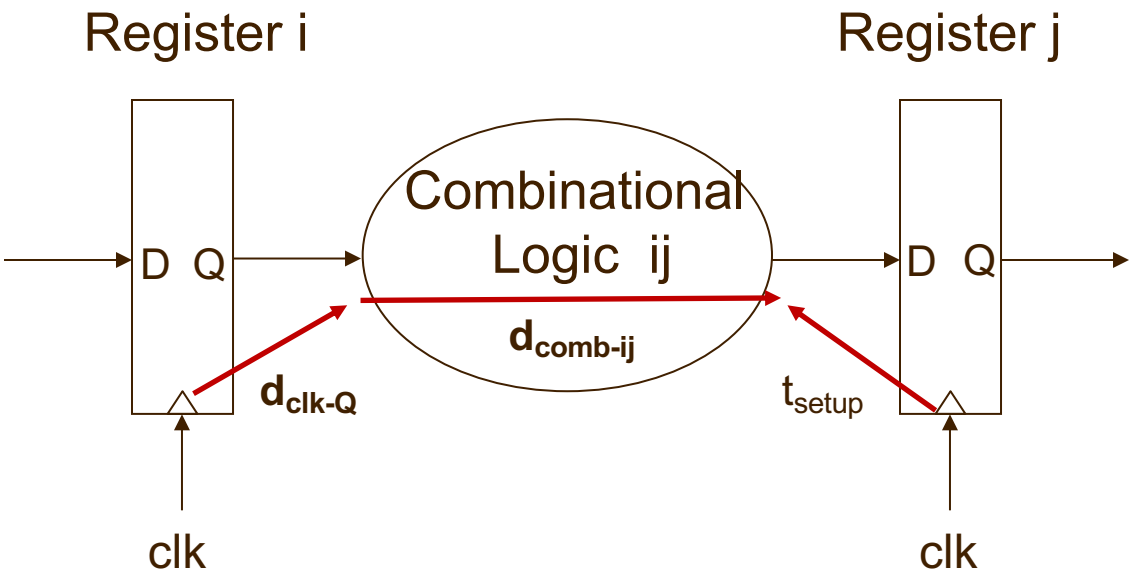
Impact on Downstream Circuitry



Timing Analysis



Path Between Two Adjacent Registers

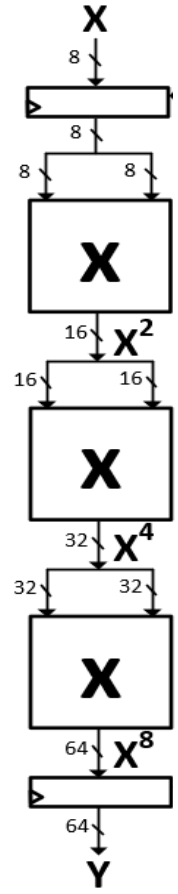


Constraint File

```
create_clock -period 10 -name clk -waveform {0.000 5.000} [get_ports clk]
```

Combinational Power Unit

Block Diagram



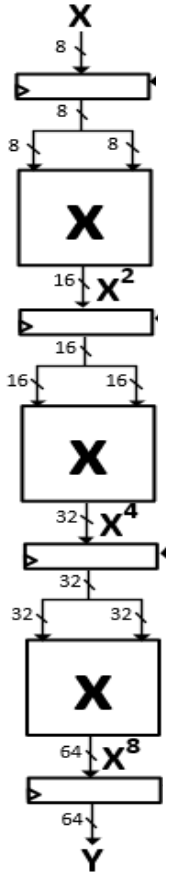
Timing report for target clock period = 10 ns

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-7.366 ns	Worst Hold Slack (WHS):	1.713 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	-1271.695 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	192	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	192	Total Number of Endpoints:	192	Total Number of Endpoints:	45

Timing constraints are not met.

Pipelined Power Unit

Block Diagram

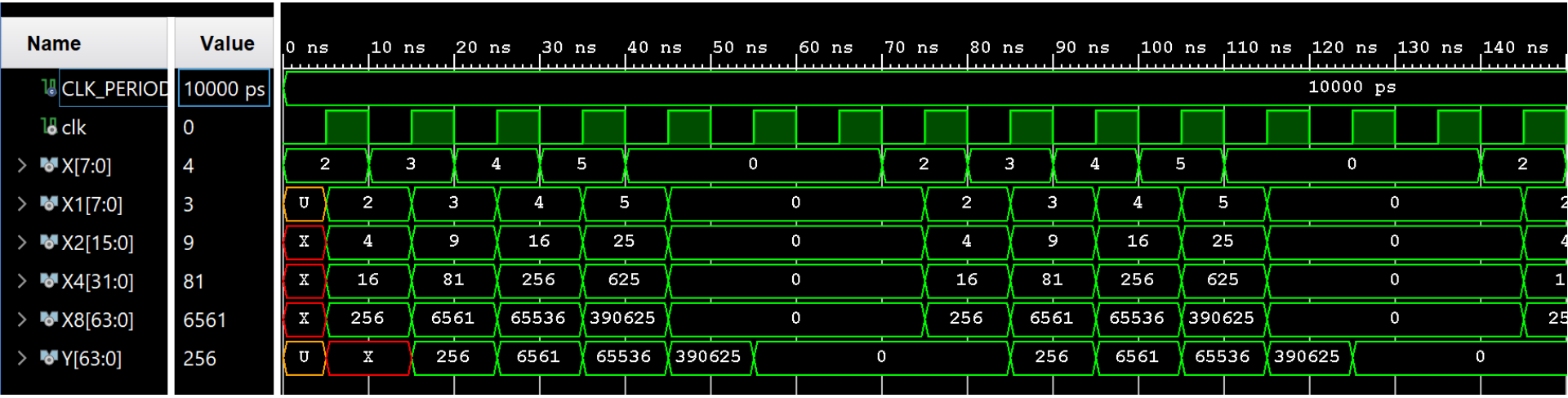


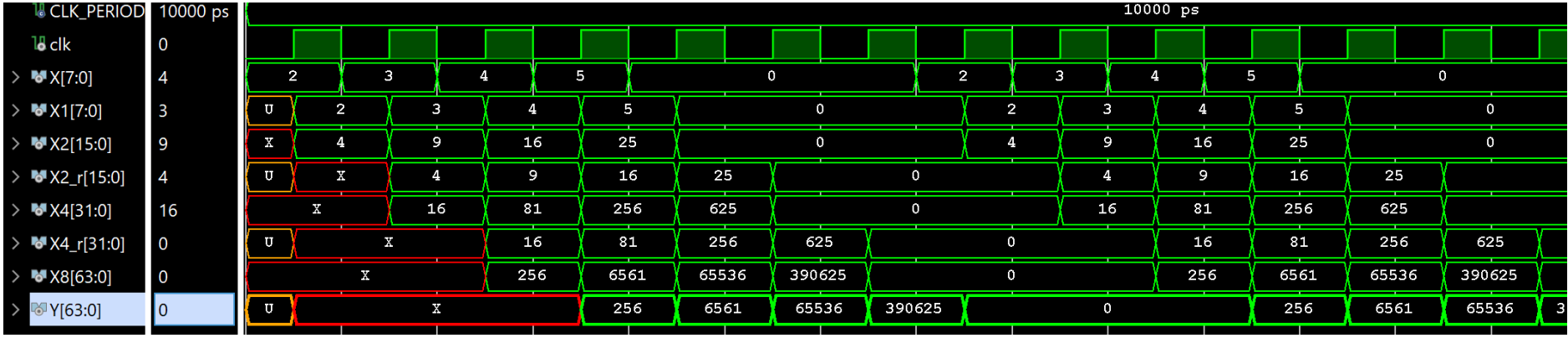
Timing report for target clock period = 10 ns

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.322 ns	Worst Hold Slack (WHS):	0.305 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	222	Total Number of Endpoints:	222	Total Number of Endpoints:	46

All user specified timing constraints are met.

Combinational Power Unit



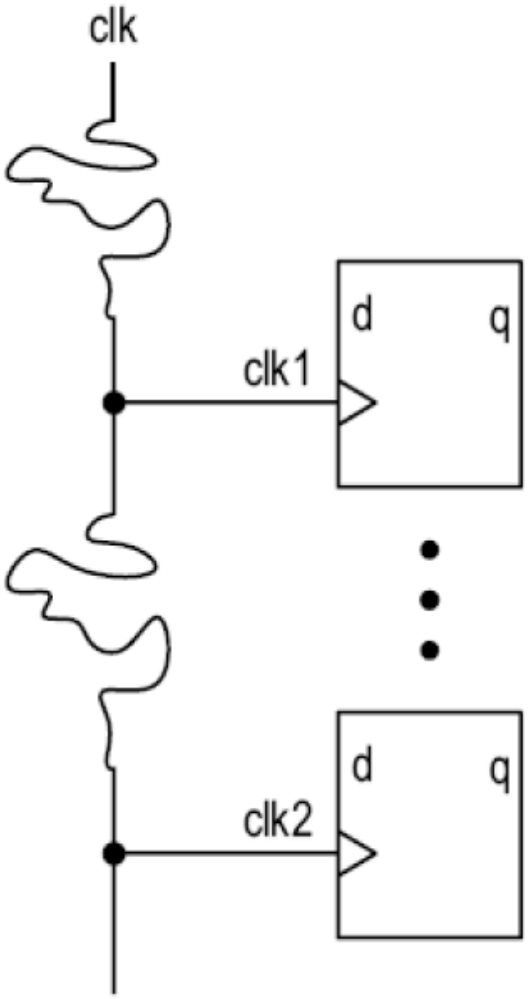


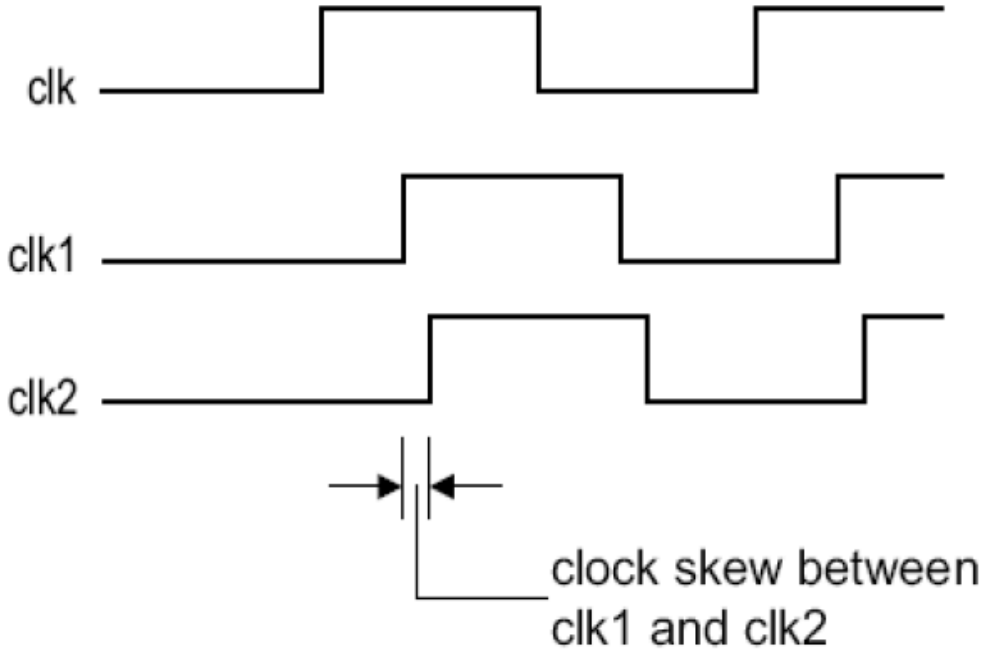
Pipelined Power Unit



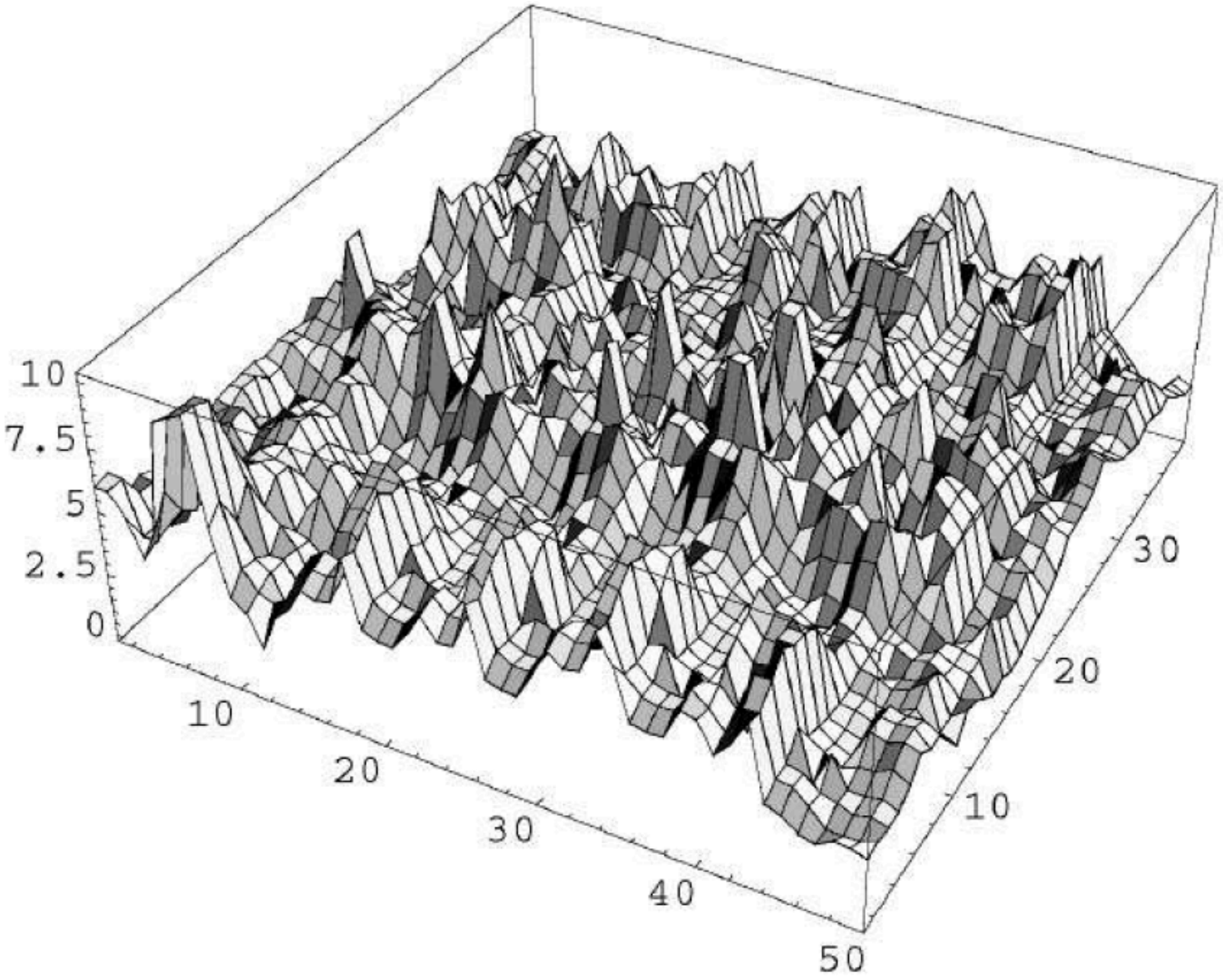
Clock Skew

Clock Skew

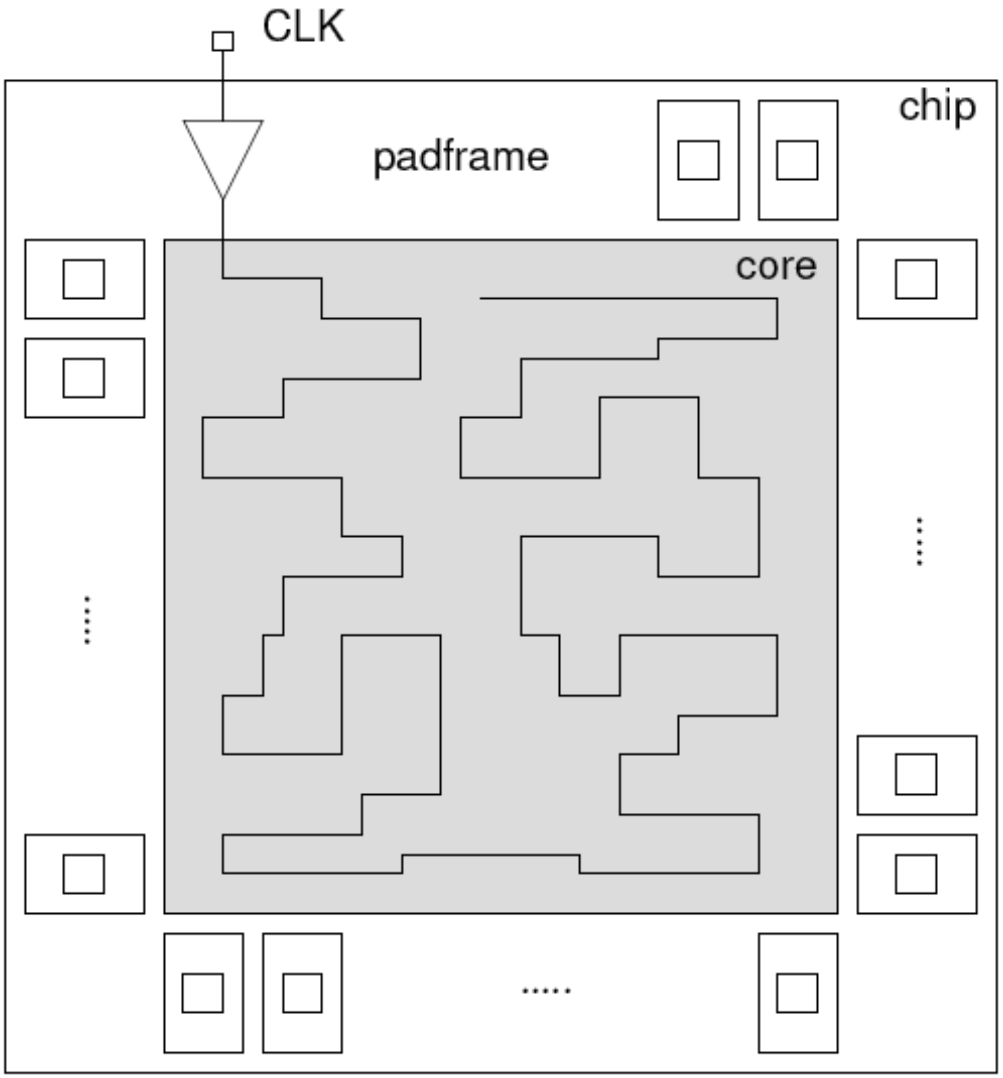

clk
d
q
clk1
d
q
clk2


clk
clk1
clk2
clock skew between
clk1 and clk2

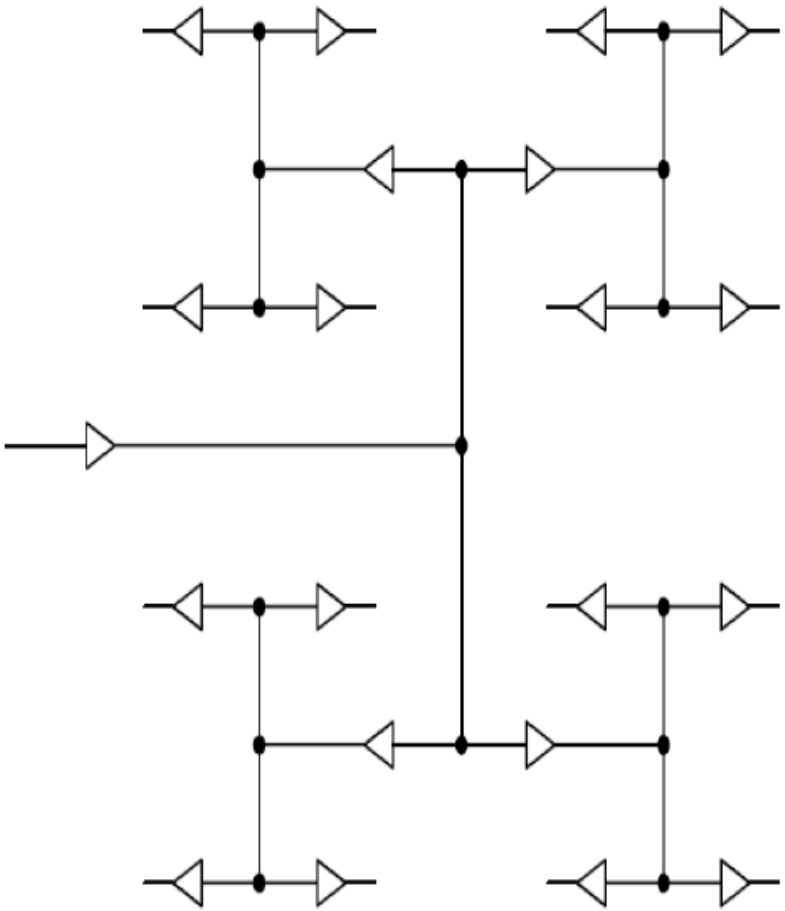
Clock Skew Map for a Cell Processor



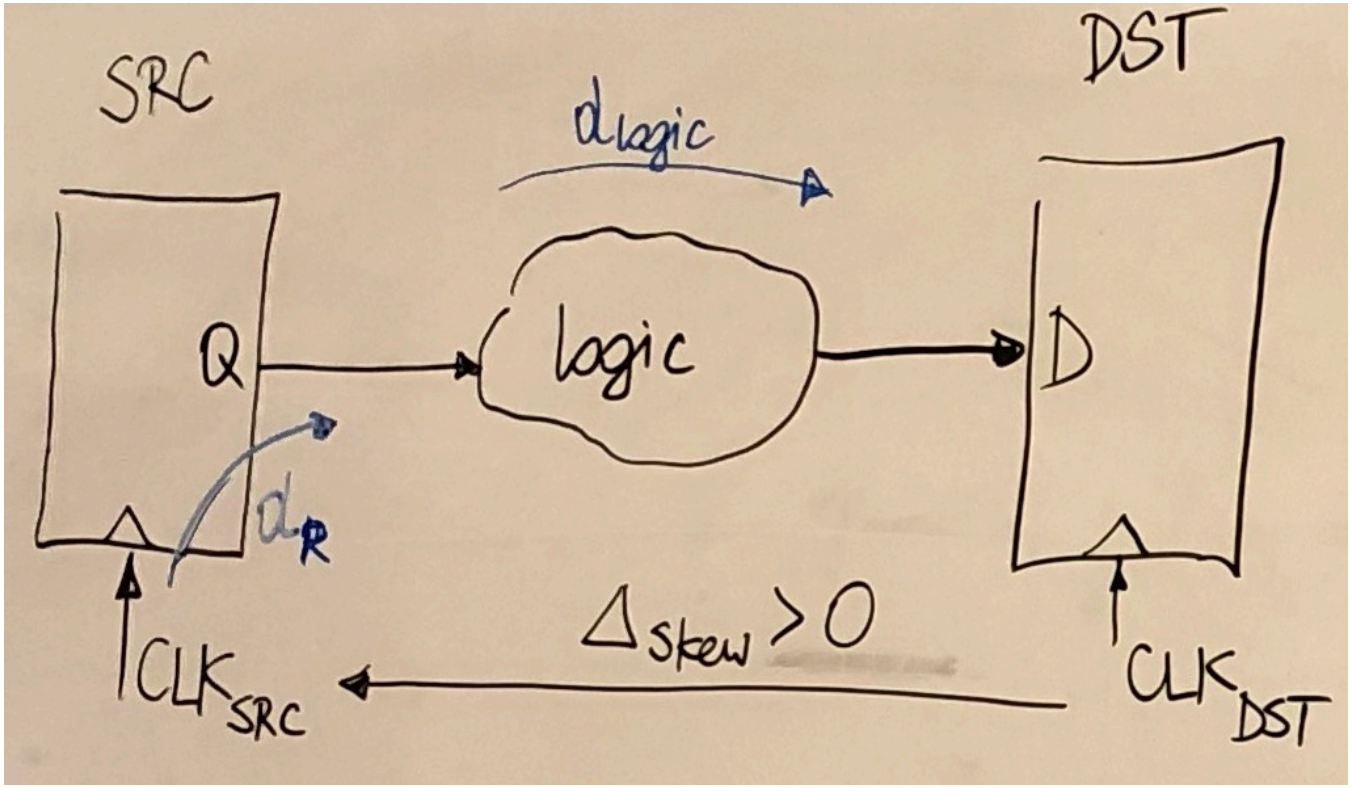
Incorrect Clock Tree Layout – Narrow Meander



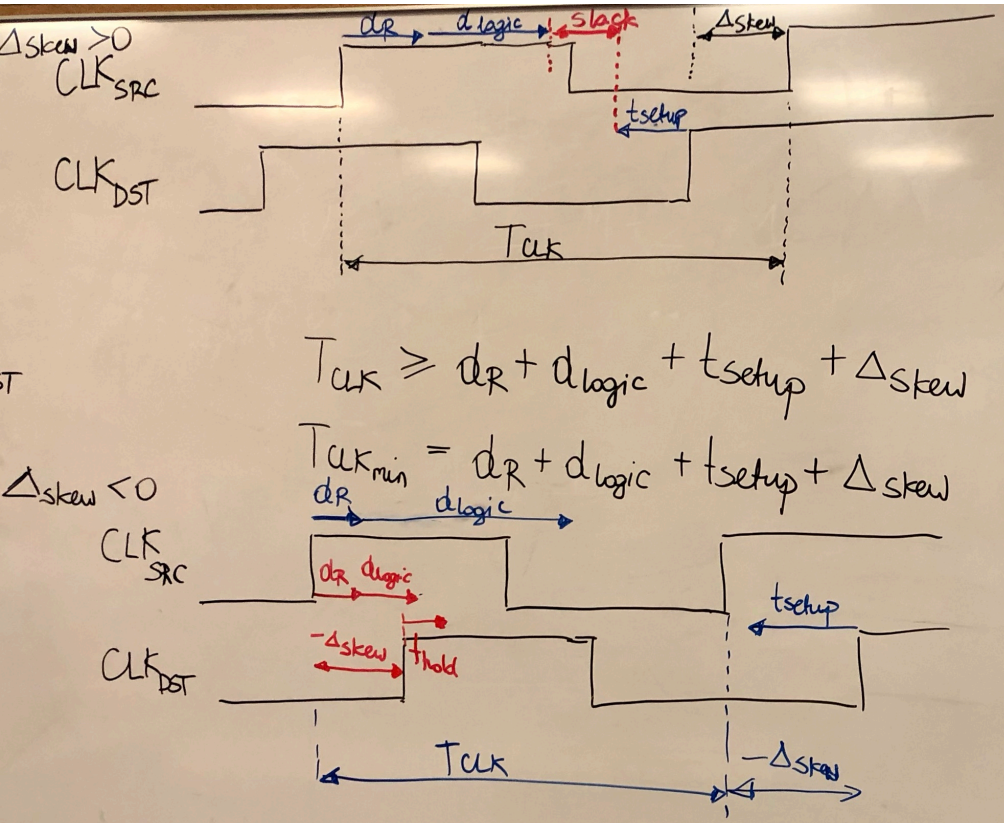
Optimized Clock Tree Layout – H Tree



Path Between Two Adjacent Registers



Timing Analysis Including Clock Skew



$T_{CLK_{min\ ij}}$

i = SRC
j = DST

$T_{CLK} \geq T_{CLK_{min\ ij}}$ for all i, j

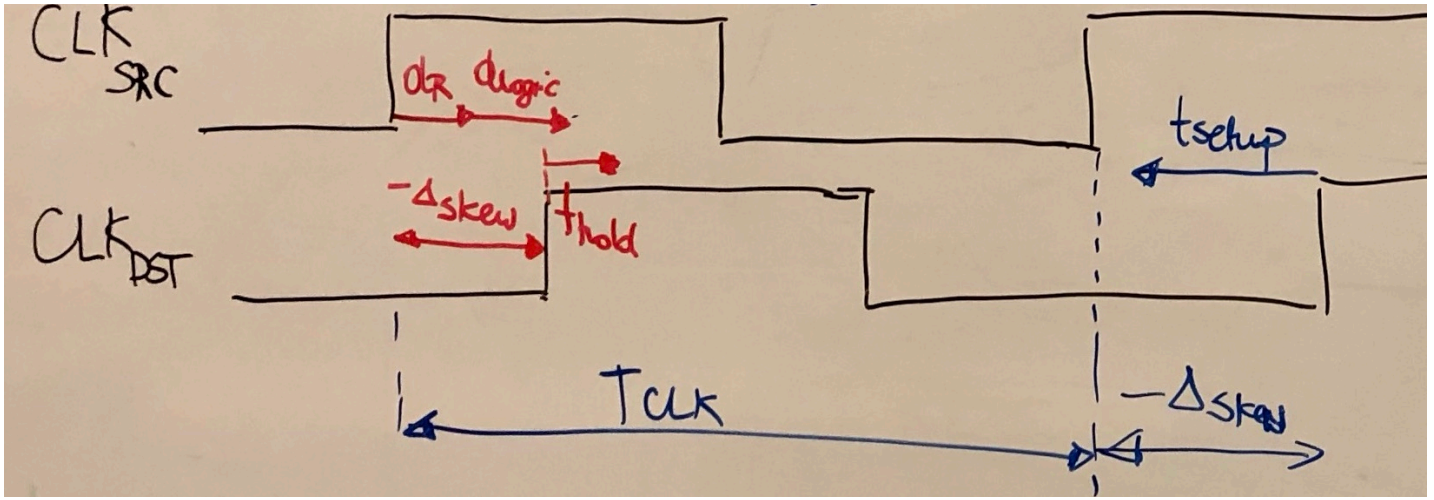
$T_{CLK_{min}} = \max \left\{ T_{CLK_{min\ ij}} \right\}$

$T_{CLK} + (-\Delta_{skew}) \geq d_R + d_{logic} + t_{setup}$

$T_{CLK} \geq d_R + d_{logic} + t_{setup} + \Delta_{skew}$

$T_{CLK_{min}} = d_R + d_{logic} + t_{setup} + \Delta_{skew}$

Hold Time Requirement



$$-\Delta_{skew} + t_{hold} \leq d_R + d_{logic}$$

$$t_{hold} \leq d_R + d_{logic} + \Delta_{skew}$$

Clock Skew - Summary

- Clock skew normally has negative impact on synchronous sequential circuit
- Effect on setup time constraint: require to increase clock period (i.e., reduce clock rate)
- Effect on hold time constraint: may introduce hold time violation
  - Can only be fixed during physical synthesis: re-route clock; re-place register and comb logic; add artificial delay logic
- Skew within 10% of clock period tolerable