ECE 545
Lecture 13

Timing Analysis

George Mason University

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Required reading

- P. Chu, *RTL Hardware Design using VHDL*

Chapter 8.6 Timing Analysis of a Synchronous Sequential Circuit

Chapter 16.1 Overview of a Clock Distribution Network

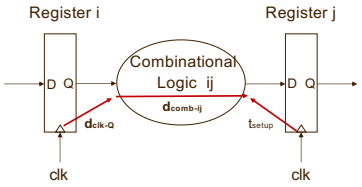
Chapter 16.2 Timing Analysis with Clock Skew

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Hold & Setup Time

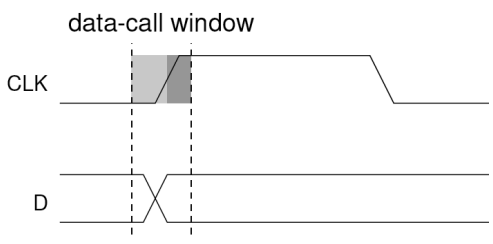
3

Path Between Two Adjacent Registers



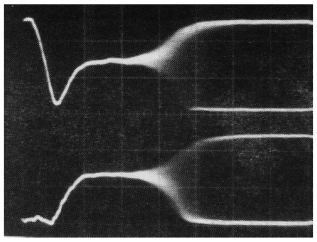
4

Violation of Hold or Setup Time



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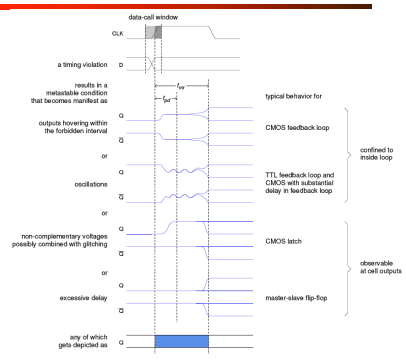
Response of a Flip-Flop to Timing Violation



There exists a third and unstable point of equilibrium between the two stable states representing the binary states 0 and 1 respectively.

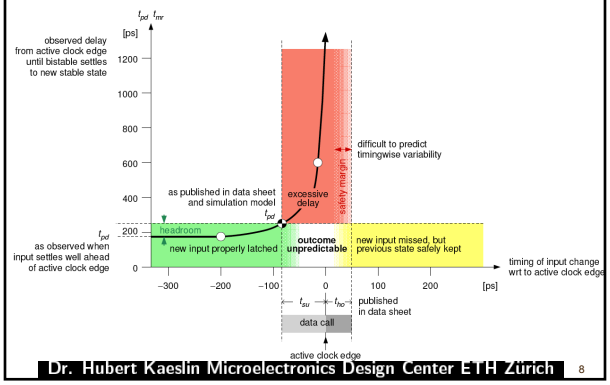
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Patterns of Metastable Behavior



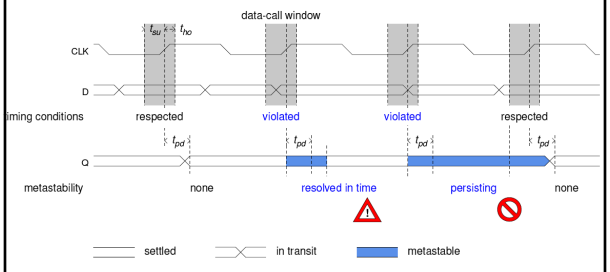
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Response to Timing Violation



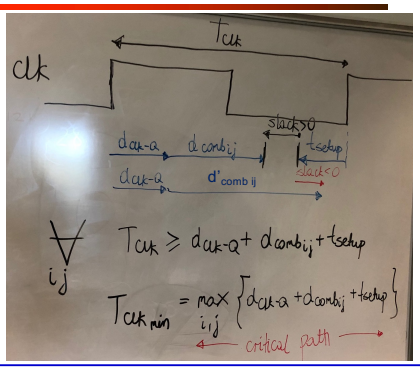
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Impact on Downstream Circuitry



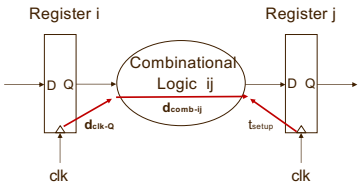
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Timing Analysis



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Path Between Two Adjacent Registers



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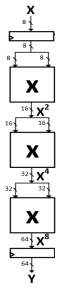
Constraint File

```
create_clock -period 10 -name clk -waveform {0.000 5.000} [get_ports clk]
```


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Combinational Power Unit

Block Diagram



Timing report for target clock period = 10 ns

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	-7.366 ns	Worst Hold Slack (WHS):	1.713 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	-1271.695 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	192	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	192	Total Number of Endpoints:	192	Total Number of Endpoints:	45

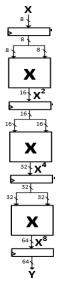
Timing constraints are not met.

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Pipelined Power Unit

Block Diagram



Timing report for target clock period = 10 ns

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2.322 ns	Worst Hold Slack (WHS):	0.305 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	222	Total Number of Endpoints:	222	Total Number of Endpoints:	46

All user specified timing constraints are met.

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Combinational Power Unit



Pipelined Power Unit

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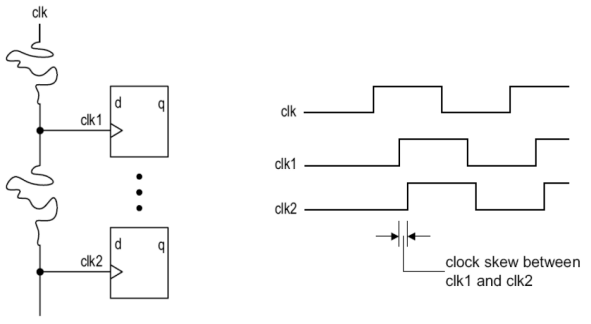
15



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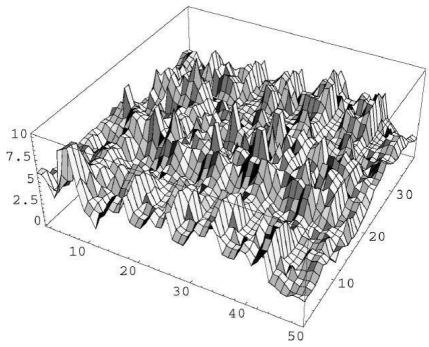
Clock Skew



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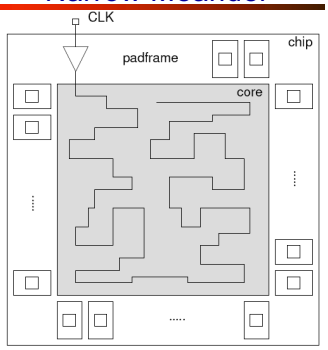
Clock Skew Map for a Cell Processor



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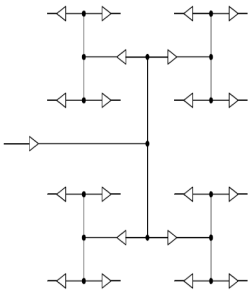
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Incorrect Clock Tree Layout – Narrow Meander



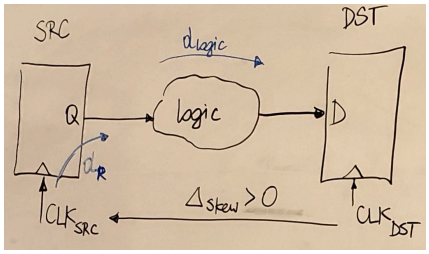
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Optimized Clock Tree Layout – H Tree



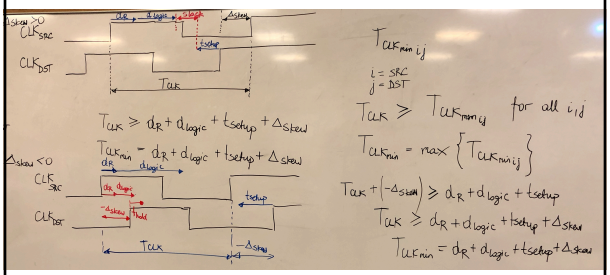
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Path Between Two Adjacent Registers



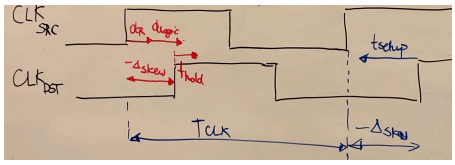
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Timing Analysis Including Clock Skew



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Hold Time Requirement



$-\Delta_{skew} + t_{hold} \leq d_R + d_{logic}$

$t_{hold} \leq d_R + d_{logic} + \Delta_{skew}$

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Clock Skew - Summary

- Clock skew normally has negative impact on synchronous sequential circuit
- Effect on setup time constraint: require to increase clock period (i.e., reduce clock rate)
- Effect on hold time constraint: may introduce hold time violation
  - Can only be fixed during physical synthesis: re-route clock; re-place register and comb logic; add artificial delay logic
- Skew within 10% of clock period tolerable

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